DCC Prototype

Design / Cost / Schedule

Eric Hazen
Jim Rohlf
Shouxiang Wu
Prototype vs Demonstrator

• 18 HTR inputs (Demonstrator has 9)
• S-Link 64 for DAQ output
  – Demonstrator has S-Link 32
• 2\textsuperscript{nd} S-Link for Trigger Data output
• Fast outputs to TTS (overflow, busy)
• More logic functionality
  – Improved Monitoring / Error Recovery
• More input bandwidth
  – 150 $\rightarrow$ 250-300 Mbytes/s/crate
DCC Prototype Architecture
Changes from Demonstrator

- No TTCRx (TTC fanout)
- Additional HTR Inputs
- Timing/Control from TTC
- DCC Logic Mezzanine Board
- Event Builder
- Output FIFOS
- Spy Memory
- Fast Monitor
- Fast signals to TTS
- Fiber to DAQ
- ? Link to Trigger Data Conc.
- S-Link LSC
- S-Link LSC
- S-Link 32 to S-Link 64
- 2nd S-Link (trig. data)
- VME-PCI Universe II
- Point-to-point Links from HTR Cards
- PCI Bus 1
- PCI Bus 2
- PCI Bus 3

6 April 2001
CMS HCAL at BU - Eric Hazen
## Bandwidth Requirements

<table>
<thead>
<tr>
<th>Detector</th>
<th>%Occ</th>
<th>QIE samples</th>
<th>32-ch HTR</th>
<th>36-ch HTR</th>
<th>L2 Filter Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>in</td>
<td>out</td>
<td>in</td>
</tr>
<tr>
<td>HB/HE</td>
<td>15%</td>
<td>10</td>
<td>281</td>
<td>175</td>
<td>310</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>259</td>
<td>158</td>
<td>288</td>
</tr>
<tr>
<td>HCAL</td>
<td>100%</td>
<td>1</td>
<td>295</td>
<td>240</td>
<td>331</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>180</td>
<td>125</td>
<td>194</td>
</tr>
</tbody>
</table>

DCC input: need 250-300 Mbytes/sec *(design upgrade)*

DCC output: < 200Mbytes/sec per TriDAS *(no problem)*

(Normal Operation)
Bandwidth Upgrade Options

- **Bandwidth Limits:**
  - PCI 1,2: 33MHz x 32 bits
    - In theory, 266 Mbytes/s
    - In reality, ~150 Mbytes/s

- **Upgrade Options:**
  1. Incremental Improvements (≤ 25%)
     - More efficient data format
     - Careful tuning of PCI bus use
  2. Major Redesign (+ 100% bw)
     - Ditch motherboard; new dedicated 9U board (3-6 month delay?)
  3. Add more DCCs where needed
     - May run out of switch inputs
     - May wreak havoc with crate/rack layouts!
     - Expensive
Prototype Development Cost

<table>
<thead>
<tr>
<th>WBS #</th>
<th>Description</th>
<th>Project M&amp;S</th>
<th>Project EDIA</th>
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<tbody>
<tr>
<td>2.1.7.3.4.1</td>
<td>DCC Prototype Design+Test</td>
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<td>$32k</td>
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<tr>
<td>2.1.7.3.4.2</td>
<td>DCC Prototype M&amp;S</td>
<td>$20k</td>
<td></td>
</tr>
</tbody>
</table>

This estimate is still valid and includes:

- New prototype 9U Motherboard with some redesign
- New prototype logic board with with some redesign

This estimate is about 50% low for a complete redesign (if needed)

_N.B. – Production DCC cost estimate is now $4.5k (WBS=$7.5k)_
DCC Prototype Schedule

• Original schedule:
  – Jan 2001 – Jan 2002 (development and testing)

• Current schedule:
  – Start: behind ~6 mo (July 2001)
    • Can make up a lot of time if no major redesign
  – Could still get back on schedule
# Approximate Costs

for various bandwidth upgrade options

<table>
<thead>
<tr>
<th>Speed Mbytes/s</th>
<th>One-time Cost</th>
<th>Production Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add a third input bus</td>
<td>225-250</td>
<td>20d engr ($6k) ML PCB Rev ($4.5k)</td>
</tr>
<tr>
<td>Reduce overhead</td>
<td>200/300</td>
<td>20d engr ($6k)</td>
</tr>
<tr>
<td>Point-to-Point from each LRB</td>
<td>450</td>
<td>30d engr ($9k) MB PCB Rev ($4.5k) Logic PCB Rev ($2.5k)</td>
</tr>
<tr>
<td>Add more DCC modules</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>

Project has $32k (100d engr) plus $20k M&S for DCC Prototype