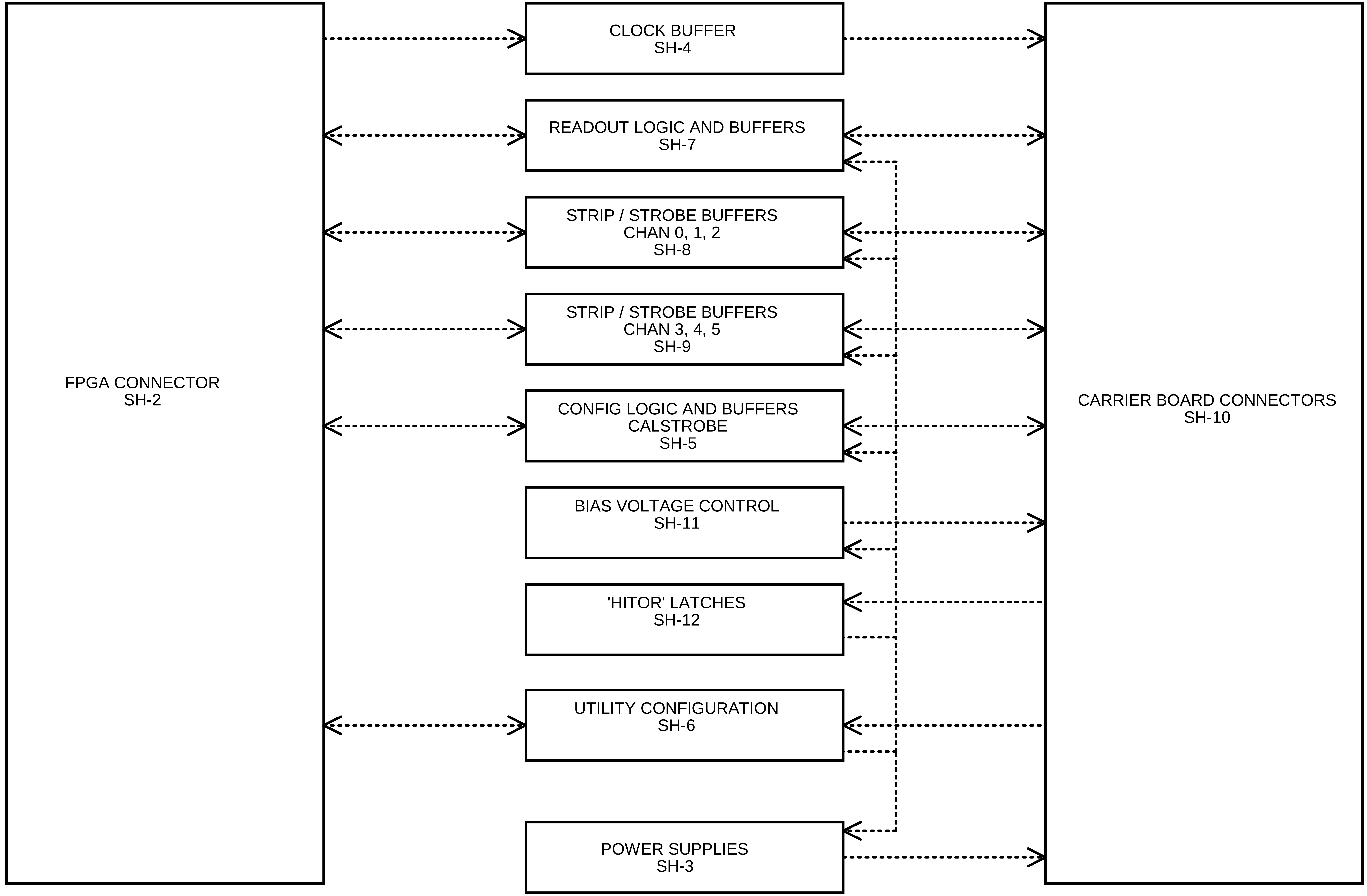
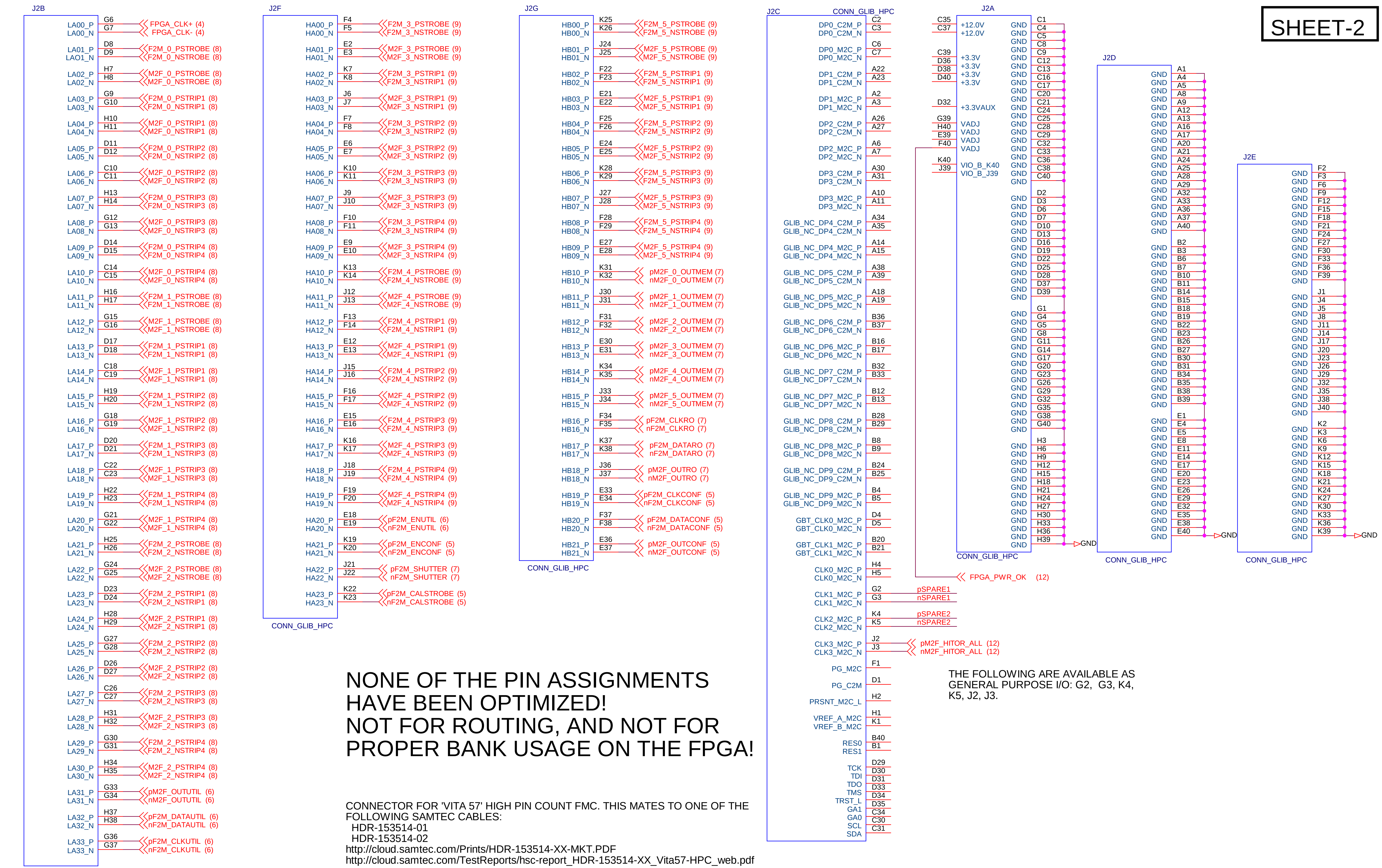


MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: BLOCK DIAGRAM		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 1 of 12	

SHEET-2



NONE OF THE PIN ASSIGNMENTS HAVE BEEN OPTIMIZED!
NOT FOR ROUTING, AND NOT FOR PROPER BANK USAGE ON THE FPGA!

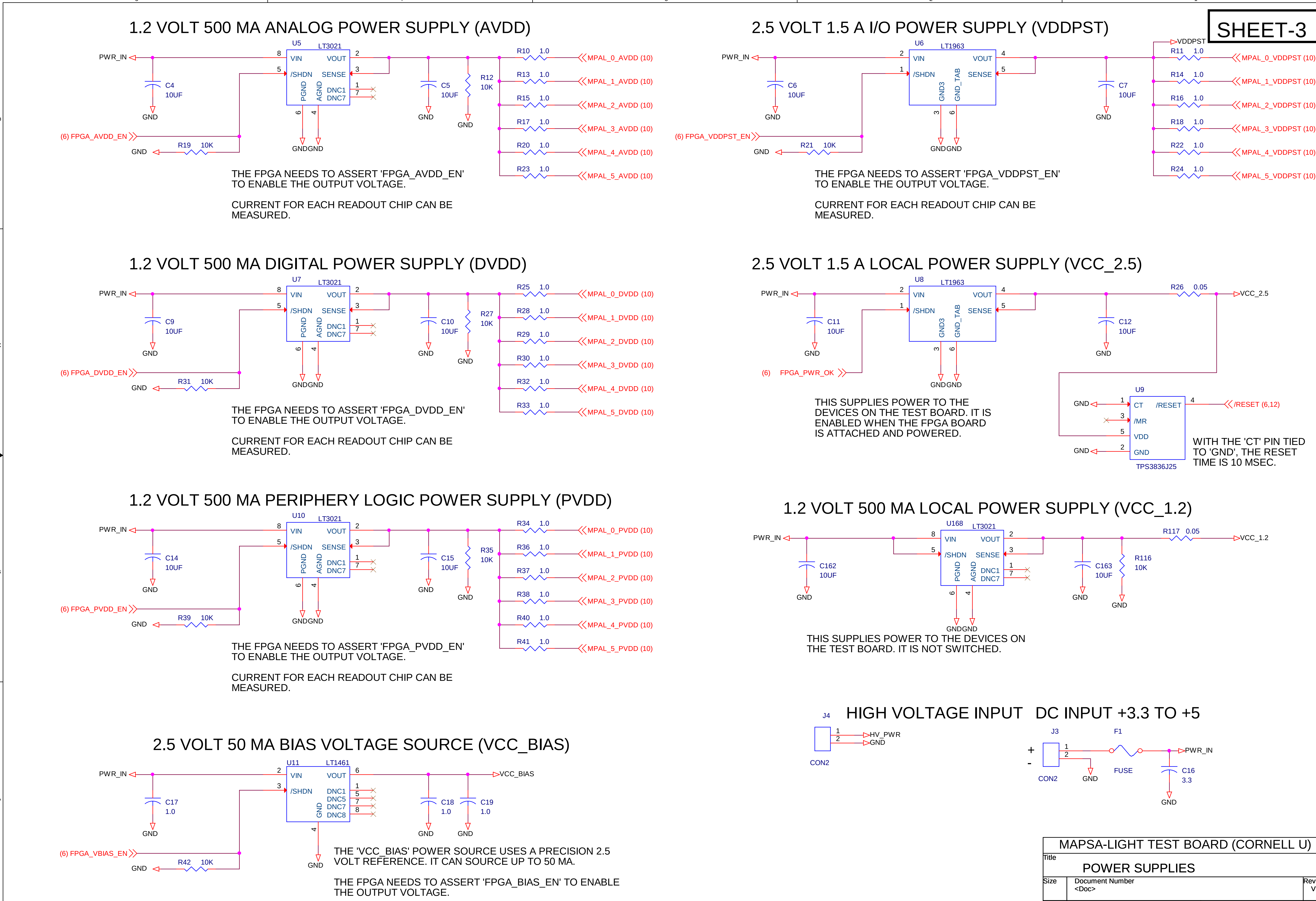
CONNECTOR FOR 'VITA 57' HIGH PIN COUNT FMC. THIS MATES TO ONE OF THE FOLLOWING SAMTEC CABLES:
HDR-153514-01
HDR-153514-02
http://cloud.samtec.com/Prints/HDR-153514-XX-MKT.PDF
http://cloud.samtec.com/TestReports/hsc-report_HDR-153514-XX_Vita57-HPC_web.pdf

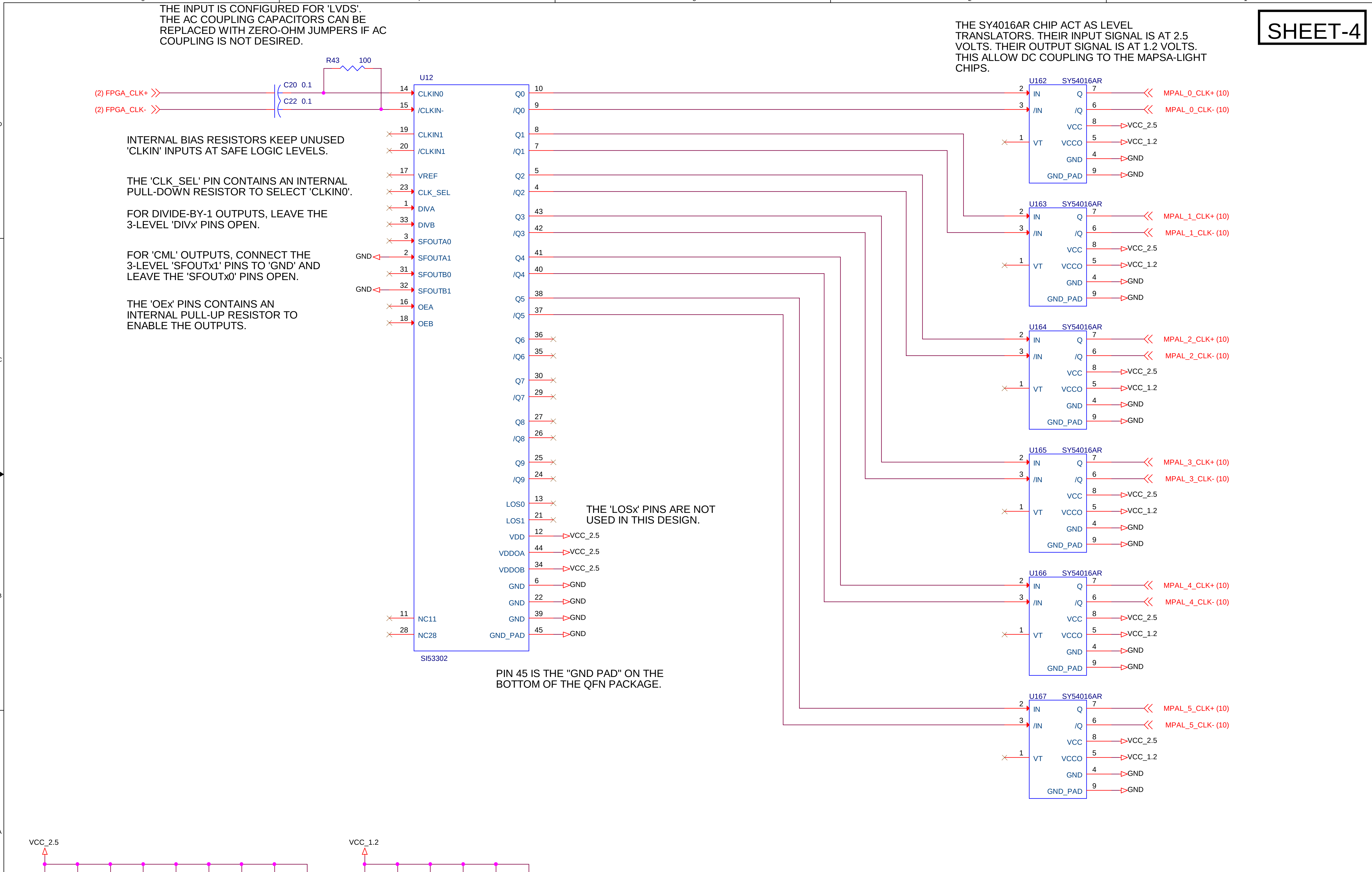
THE FOLLOWING ARE AVAILABLE AS GENERAL PURPOSE I/O: G2, G3, K4, K5, J2, J3.

HOLES FOR MOUNTING THE VITA-57 CONNECTOR

HOLES FOR SUPPORTING THE BOARD.

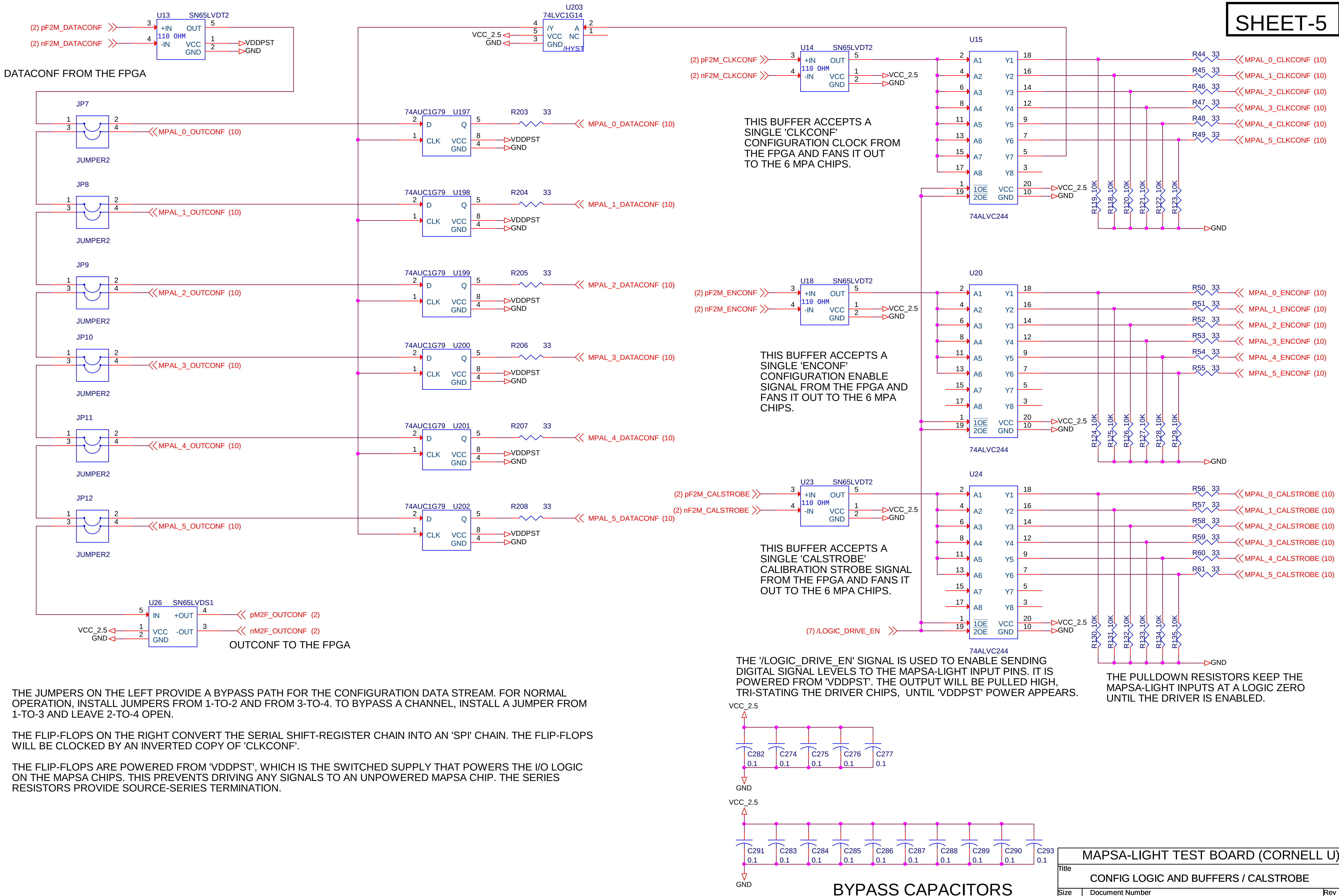
	MAPSA-LIGHT TEST BOARD (CORNELL U)
Title	FPGA CONNECTOR
Size	Document Number <Doc> — Rev V2
Date:	Wednesday, June 17, 2015 — Sheet 2 of 12


SHEET-3
1.2 VOLT 500 MA ANALOG POWER SUPPLY (AVDD)
U5 LT3021 VIN VOUT /SHDN SENSE PGND AGND DNC1 DNC7
PWR_IN C4 10UF GND
(6) FPGA_AVDD_EN
R19 10K
C5 10UF R12 10K
R10 1.0 MPAL_0_AVDD (10)
R13 1.0 MPAL_1_AVDD (10)
R15 1.0 MPAL_2_AVDD (10)
R17 1.0 MPAL_3_AVDD (10)
R20 1.0 MPAL_4_AVDD (10)
R23 1.0 MPAL_5_AVDD (10)
THE FPGA NEEDS TO ASSERT 'FPGA_AVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.
CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.
2.5 VOLT 1.5 A I/O POWER SUPPLY (VDDPST)
U6 LT1963 VIN VOUT /SHDN SENSE GND3 GND_TAB
PWR_IN C6 10UF GND
(6) FPGA_VDDPST_EN
R21 10K
C7 10UF
VDDPST
R11 1.0 MPAL_0_VDDPST (10)
R14 1.0 MPAL_1_VDDPST (10)
R16 1.0 MPAL_2_VDDPST (10)
R18 1.0 MPAL_3_VDDPST (10)
R22 1.0 MPAL_4_VDDPST (10)
R24 1.0 MPAL_5_VDDPST (10)
THE FPGA NEEDS TO ASSERT 'FPGA_VDDPST_EN' TO ENABLE THE OUTPUT VOLTAGE.
CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.
1.2 VOLT 500 MA DIGITAL POWER SUPPLY (DVDD)
U7 LT3021 VIN VOUT /SHDN SENSE PGND AGND DNC1 DNC7
PWR_IN C9 10UF GND
(6) FPGA_DVDD_EN
R31 10K
C10 10UF R27 10K
R25 1.0 MPAL_0_DVDD (10)
R28 1.0 MPAL_1_DVDD (10)
R29 1.0 MPAL_2_DVDD (10)
R30 1.0 MPAL_3_DVDD (10)
R32 1.0 MPAL_4_DVDD (10)
R33 1.0 MPAL_5_DVDD (10)
THE FPGA NEEDS TO ASSERT 'FPGA_DVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.
CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.
2.5 VOLT 1.5 A LOCAL POWER SUPPLY (VCC_2.5)
U8 LT1963 VIN VOUT /SHDN SENSE GND3 GND_TAB
PWR_IN C11 10UF GND
(6) FPGA_PWR_OK
C12 10UF
R26 0.05 VCC_2.5
U9 TPS3836J25 CT /RESET /MR VDD GND
/RESET (6,12)
THIS SUPPLIES POWER TO THE DEVICES ON THE TEST BOARD. IT IS ENABLED WHEN THE FPGA BOARD IS ATTACHED AND POWERED.
WITH THE 'CT' PIN TIED TO 'GND', THE RESET TIME IS 10 MSEC.
1.2 VOLT 500 MA PERIPHERY LOGIC POWER SUPPLY (PVDD)
U10 LT3021 VIN VOUT /SHDN SENSE PGND AGND DNC1 DNC7
PWR_IN C14 10UF GND
(6) FPGA_PVDD_EN
R39 10K
C15 10UF R35 10K
R34 1.0 MPAL_0_PVDD (10)
R36 1.0 MPAL_1_PVDD (10)
R37 1.0 MPAL_2_PVDD (10)
R38 1.0 MPAL_3_PVDD (10)
R40 1.0 MPAL_4_PVDD (10)
R41 1.0 MPAL_5_PVDD (10)
THE FPGA NEEDS TO ASSERT 'FPGA_PVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.
CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.
1.2 VOLT 500 MA LOCAL POWER SUPPLY (VCC_1.2)
U168 LT3021 VIN VOUT /SHDN SENSE PGND AGND DNC1 DNC7
PWR_IN C162 10UF GND
C163 10UF R116 10K
R117 0.05 VCC_1.2
THIS SUPPLIES POWER TO THE DEVICES ON THE TEST BOARD. IT IS NOT SWITCHED.
2.5 VOLT 50 MA BIAS VOLTAGE SOURCE (VCC_BIAS)
U11 LT1461 VIN VOUT /SHDN GND DNC1 DNC5 DNC7 DNC8
PWR_IN C17 1.0 GND
(6) FPGA_VBIAS_EN
R42 10K
C18 1.0 C19 1.0 VCC_BIAS
THE 'VCC_BIAS' POWER SOURCE USES A PRECISION 2.5 VOLT REFERENCE. IT CAN SOURCE UP TO 50 MA.
THE FPGA NEEDS TO ASSERT 'FPGA_BIAS_EN' TO ENABLE THE OUTPUT VOLTAGE.
HIGH VOLTAGE INPUT
J4 CON2 HV_PWR GND
DC INPUT +3.3 TO +5
J3 CON2 + -
F1 FUSE PWR_IN
C16 3.3 GND
MAPSA-LIGHT TEST BOARD (CORNELL U)
Title POWER SUPPLIES
Size Document Number <Doc> Rev V2
Date: Wednesday, June 17, 2015 Sheet 3 of 12



MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: CLOCK BUFFERS		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 4 of 12	

SHEET-5



THE JUMPERS ON THE LEFT PROVIDE A BYPASS PATH FOR THE CONFIGURATION DATA STREAM. FOR NORMAL OPERATION, INSTALL JUMPERS FROM 1-TO-2 AND FROM 3-TO-4. TO BYPASS A CHANNEL, INSTALL A JUMPER FROM 1-TO-3 AND LEAVE 2-TO-4 OPEN.

THE FLIP-FLOPS ON THE RIGHT CONVERT THE SERIAL SHIFT-REGISTER CHAIN INTO AN 'SPI' CHAIN. THE FLIP-FLOPS WILL BE CLOCKED BY AN INVERTED COPY OF 'CLKCONF'.

THE FLIP-FLOPS ARE POWERED FROM 'VDDPST', WHICH IS THE SWITCHED SUPPLY THAT POWERS THE I/O LOGIC ON THE MAPSA CHIPS. THIS PREVENTS DRIVING ANY SIGNALS TO AN UNPOWERED MAPSA CHIP. THE SERIES RESISTORS PROVIDE SOURCE-SERIES TERMINATION.

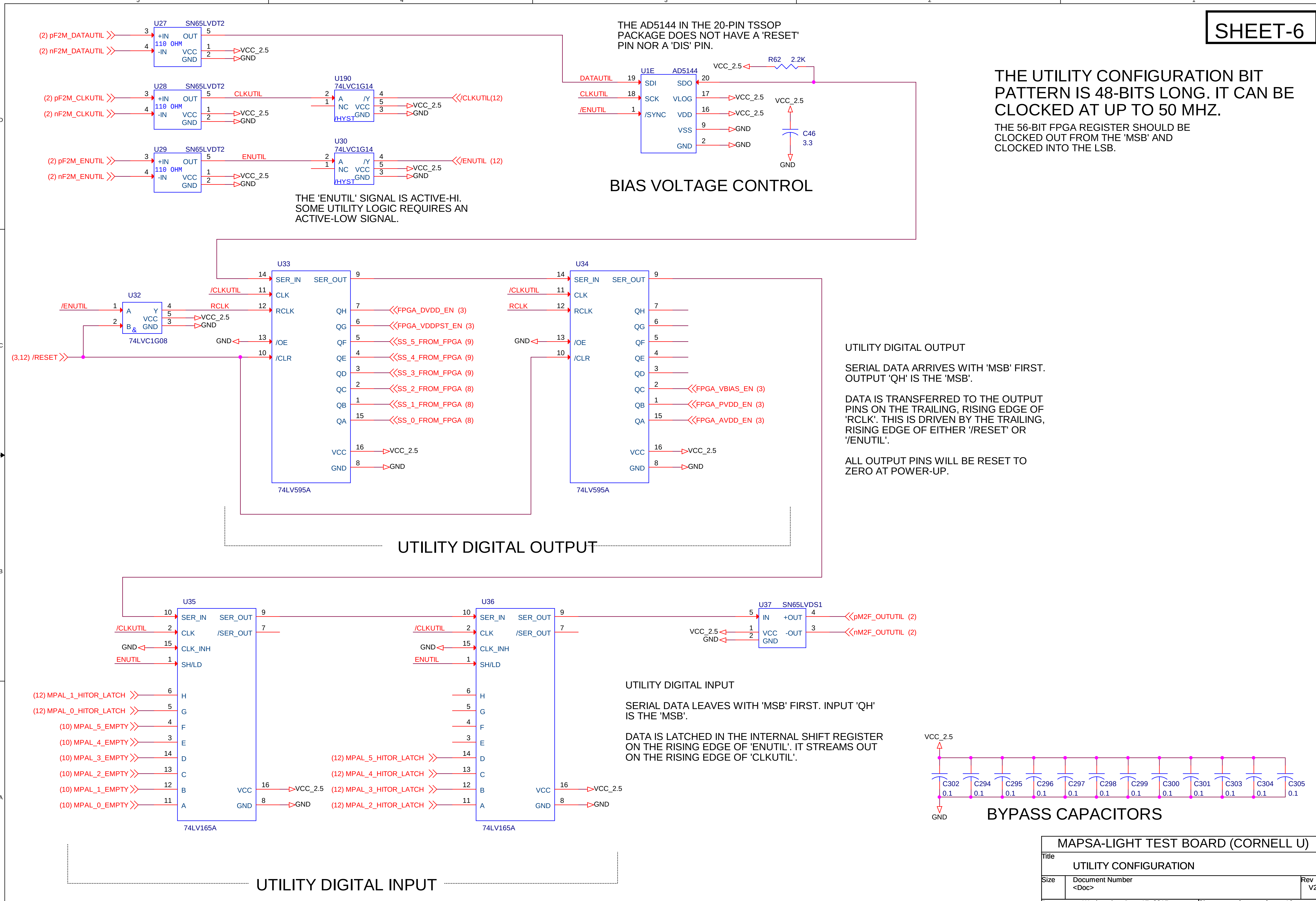
BYPASS CAPACITORS

MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: CONFIG LOGIC AND BUFFERS / CALSTROBE

Size | Document Number: <Doc> | Rev: V2

Date: Wednesday, June 17, 2015 | Sheet 5 of 12



THE AD5144 IN THE 20-PIN TSSOP PACKAGE DOES NOT HAVE A 'RESET' PIN NOR A 'DIS' PIN.

THE UTILITY CONFIGURATION BIT PATTERN IS 48-BITS LONG. IT CAN BE CLOCKED AT UP TO 50 MHZ.

THE 56-BIT FPGA REGISTER SHOULD BE CLOCKED OUT FROM THE 'MSB' AND CLOCKED INTO THE LSB.

THE 'ENUTIL' SIGNAL IS ACTIVE-HI. SOME UTILITY LOGIC REQUIRES AN ACTIVE-LOW SIGNAL.

UTILITY DIGITAL OUTPUT

SERIAL DATA ARRIVES WITH 'MSB' FIRST. OUTPUT 'QH' IS THE 'MSB'.

DATA IS TRANSFERRED TO THE OUTPUT PINS ON THE TRAILING, RISING EDGE OF 'RCLK'. THIS IS DRIVEN BY THE TRAILING, RISING EDGE OF EITHER '/RESET' OR '/ENUTIL'.

ALL OUTPUT PINS WILL BE RESET TO ZERO AT POWER-UP.

UTILITY DIGITAL INPUT

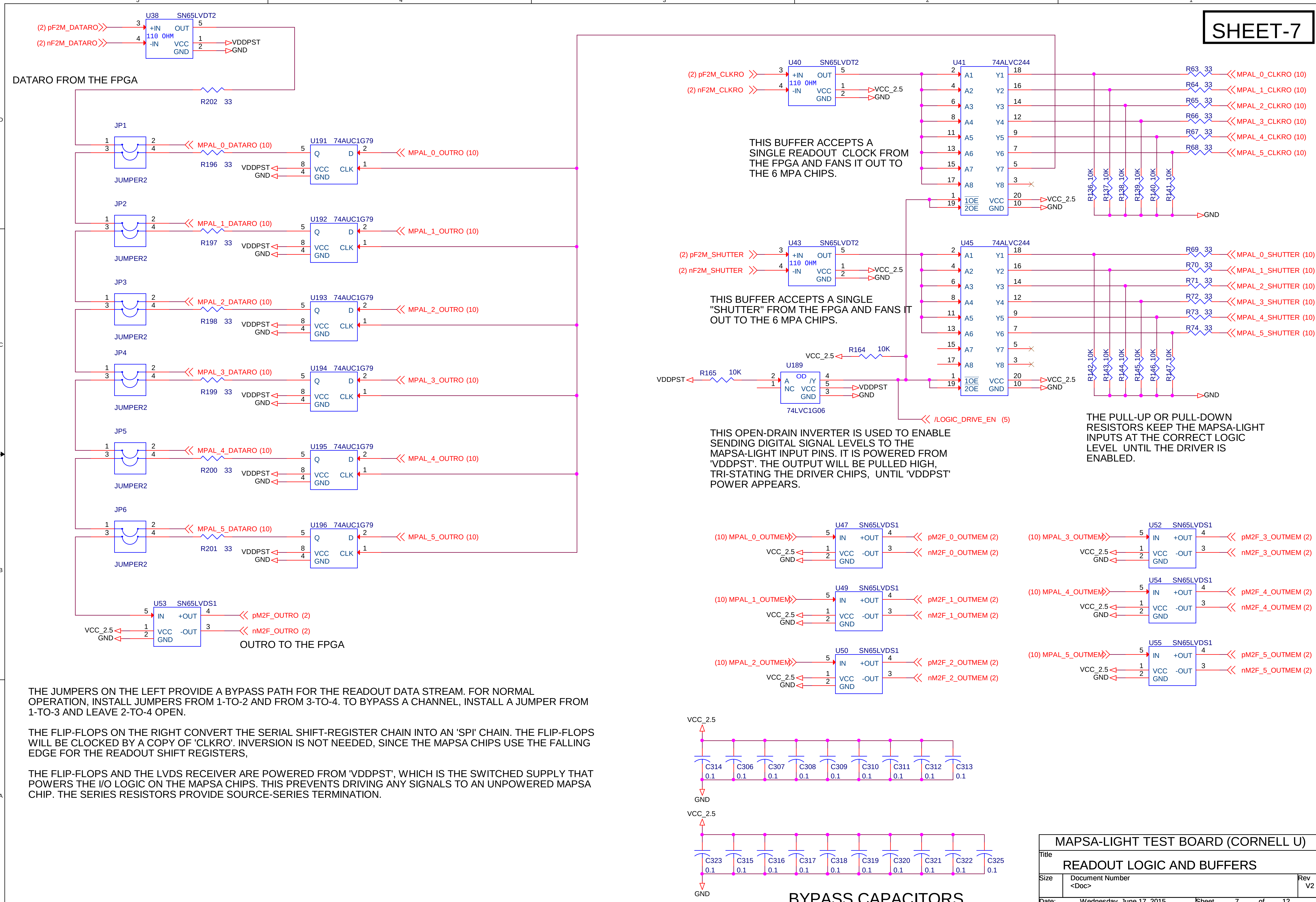
SERIAL DATA LEAVES WITH 'MSB' FIRST. INPUT 'QH' IS THE 'MSB'.

DATA IS LATCHED IN THE INTERNAL SHIFT REGISTER ON THE RISING EDGE OF 'ENUTIL'. IT STREAMS OUT ON THE RISING EDGE OF 'CLKUTIL'.

MAPSA-LIGHT TEST BOARD (CORNELL U)

Title	UTILITY CONFIGURATION
Size	Document Number <Doc> — Rev V2
Date:	Wednesday, June 17, 2015 — Sheet 6 of 12

SHEET-7



THE JUMPERS ON THE LEFT PROVIDE A BYPASS PATH FOR THE READOUT DATA STREAM. FOR NORMAL OPERATION, INSTALL JUMPERS FROM 1-TO-2 AND FROM 3-TO-4. TO BYPASS A CHANNEL, INSTALL A JUMPER FROM 1-TO-3 AND LEAVE 2-TO-4 OPEN.

THE FLIP-FLOPS ON THE RIGHT CONVERT THE SERIAL SHIFT-REGISTER CHAIN INTO AN 'SPI' CHAIN. THE FLIP-FLOPS WILL BE CLOCKED BY A COPY OF 'CLKRO'. INVERSION IS NOT NEEDED, SINCE THE MAPSA CHIPS USE THE FALLING EDGE FOR THE READOUT SHIFT REGISTERS,

THE FLIP-FLOPS AND THE LVDS RECEIVER ARE POWERED FROM 'VDDPST', WHICH IS THE SWITCHED SUPPLY THAT POWERS THE I/O LOGIC ON THE MAPSA CHIPS. THIS PREVENTS DRIVING ANY SIGNALS TO AN UNPOWERED MAPSA CHIP. THE SERIES RESISTORS PROVIDE SOURCE-SERIES TERMINATION.

MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: READOUT LOGIC AND BUFFERS		
Size	Document Number <Doc>	Rev V2
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SHEET-8

STRIP AND STROBE BUFFERING

ON THE MPA-LIGHT, STRIP AND STROBE ARE BI-DIRECTIONAL SIGNALS AT 160 MHZ. ON THE CABLE, THEY ARE UNI-DIRECTIONAL SIGNALS ON INDEPENDENT LVDS PAIRS.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE NEGATED (LOW) WHEN THE MPA-LIGHT CHIP IS SENDING DATA TO THE FPGA. THE BUFFER IS TRI-STATED IN THIS CONDITION.

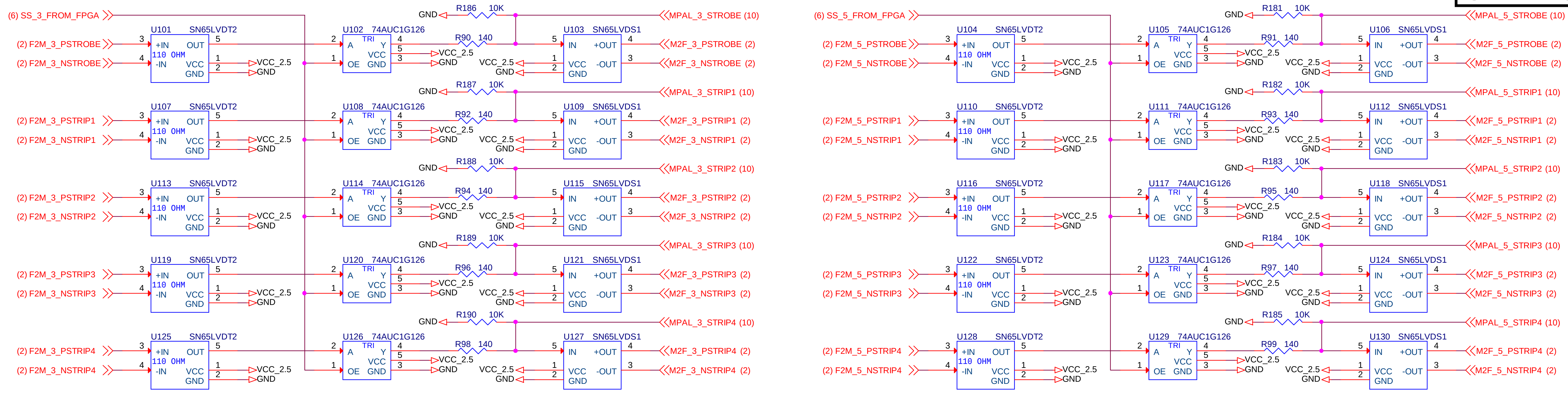
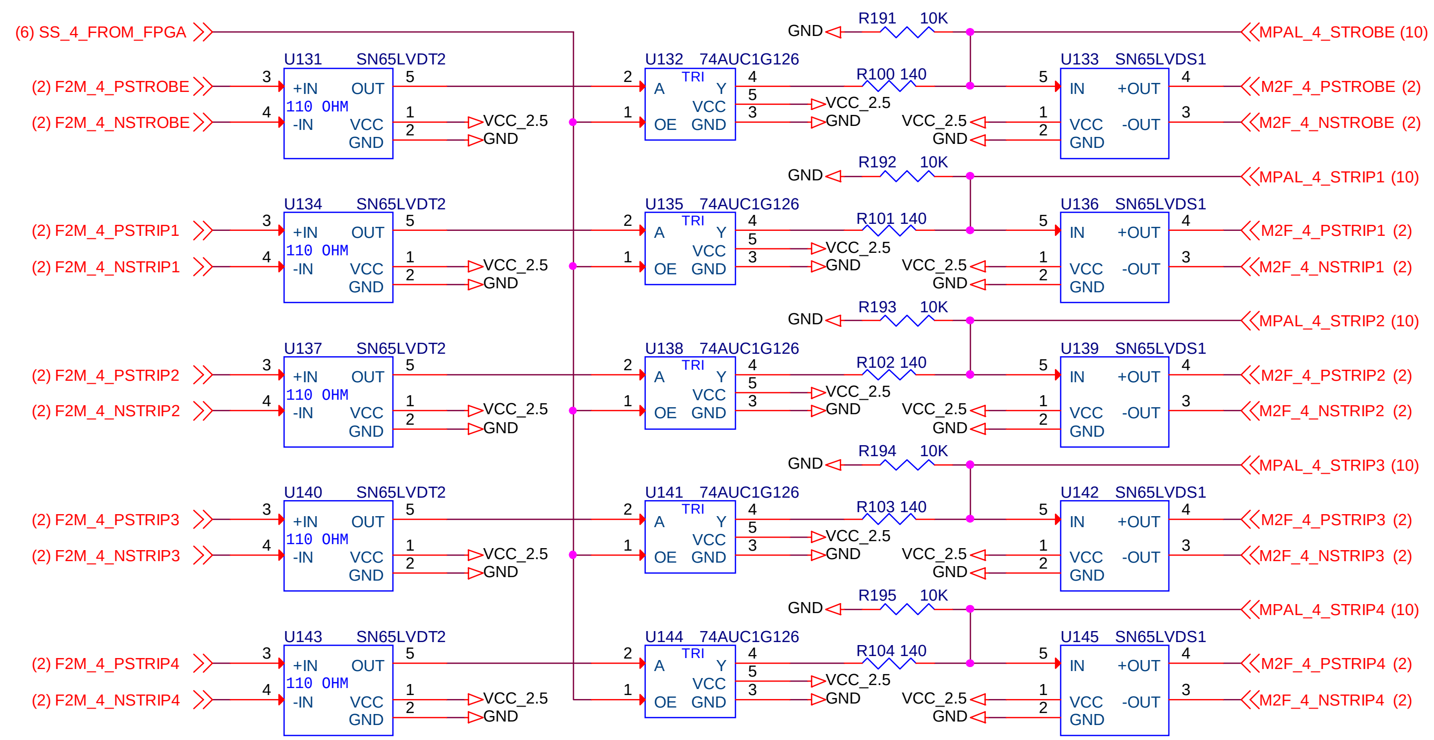
THE 'SS_x_FROM_FPGA' SIGNAL MUST BE ASSERTED (HIGH) WHEN THE MPA-LIGHT IS RECEIVING DATA FROM THE FPGA. THE BUFFER IS ENABLED IN THIS CONDITION.

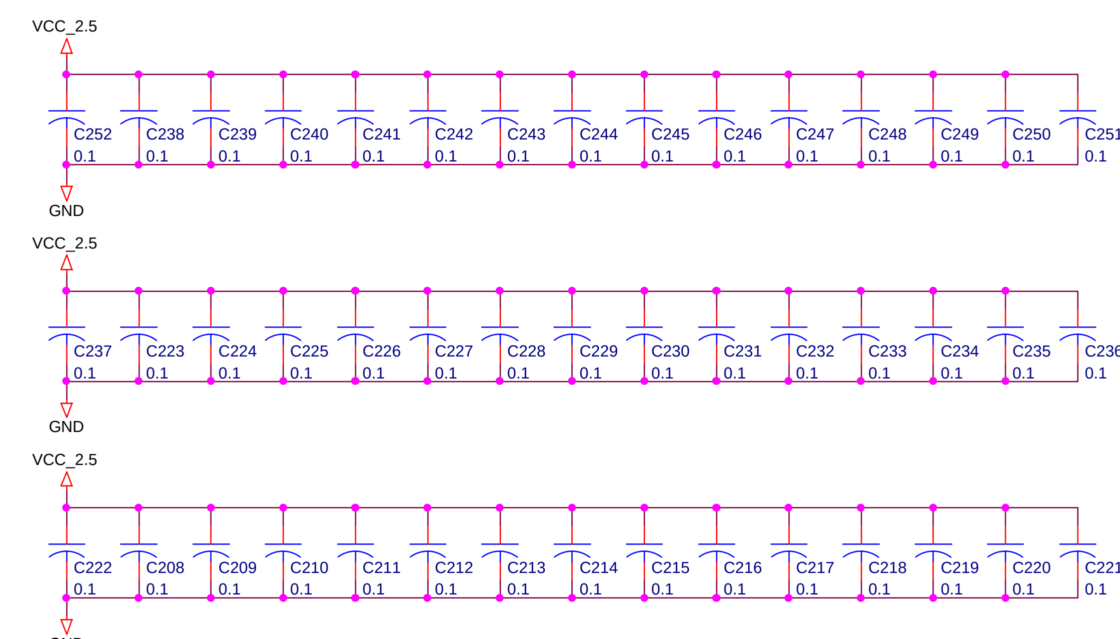
THE 'SS_x_FROM_FPGA' SIGNALS WILL ALL BE NEGATED (LOW) AT POWER-UP. THE 10K PULL-DOWN RESISTORS WILL PROVIDE A LOGIC '0'.

THE 140 OHM RESISTOR LIMITS THE MAXIMUM CURRENT THAT CAN FLOW IF BOTH DRIVERS ARE INADVERTENTLY ACTIVE.

MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: STRIP / STROBE BUFFERS 0,1,2		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 8 of 12	

SHEET-9



BYPASS CAPACITORS

STRIP AND STROBE BUFFERING

ON THE MPA-LIGHT, STRIP AND STROBE ARE BI-DIRECTIONAL SIGNALS AT 160 MHZ. ON THE CABLE, THEY ARE UNI-DIRECTIONAL SIGNALS ON INDEPENDENT LVDS PAIRS.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE NEGATED (LOW) WHEN THE MPA-LIGHT CHIP IS SENDING DATA TO THE FPGA. THE BUFFER IS TRI-STATED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE ASSERTED (HIGH) WHEN THE MPA-LIGHT IS RECEIVING DATA FROM THE FPGA. THE BUFFER IS ENABLED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNALS WILL ALL BE NEGATED (LOW) AT POWER-UP. THE 10K PULL-DOWN RESISTORS WILL PROVIDE A LOGIC '0'.

THE 140 OHM RESISTOR LIMITS THE MAXIMUM CURRENT THAT CAN FLOW IF BOTH DRIVERS ARE INADVERTENTLY ACTIVE.

MAPSA-LIGHT TEST BOARD (CORNELL U)	
Title: STRIP / STROBE BUFFERS 3,4,5	
Size / Document Number: <Doc>	Rev: V2
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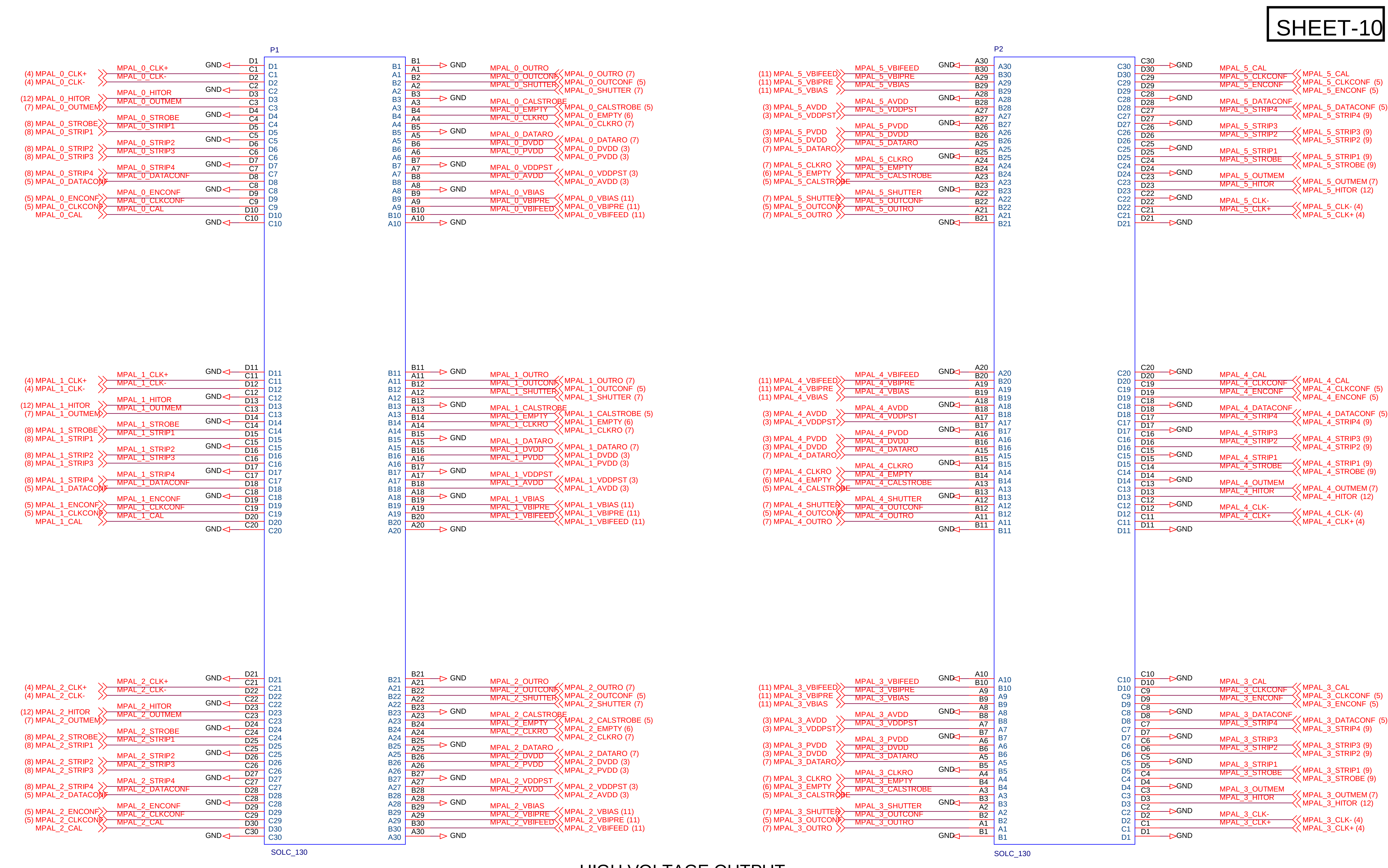

MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: CARRIER BOARD CONNECTORS		
Size	Document Number: <Doc>	Rev: V2
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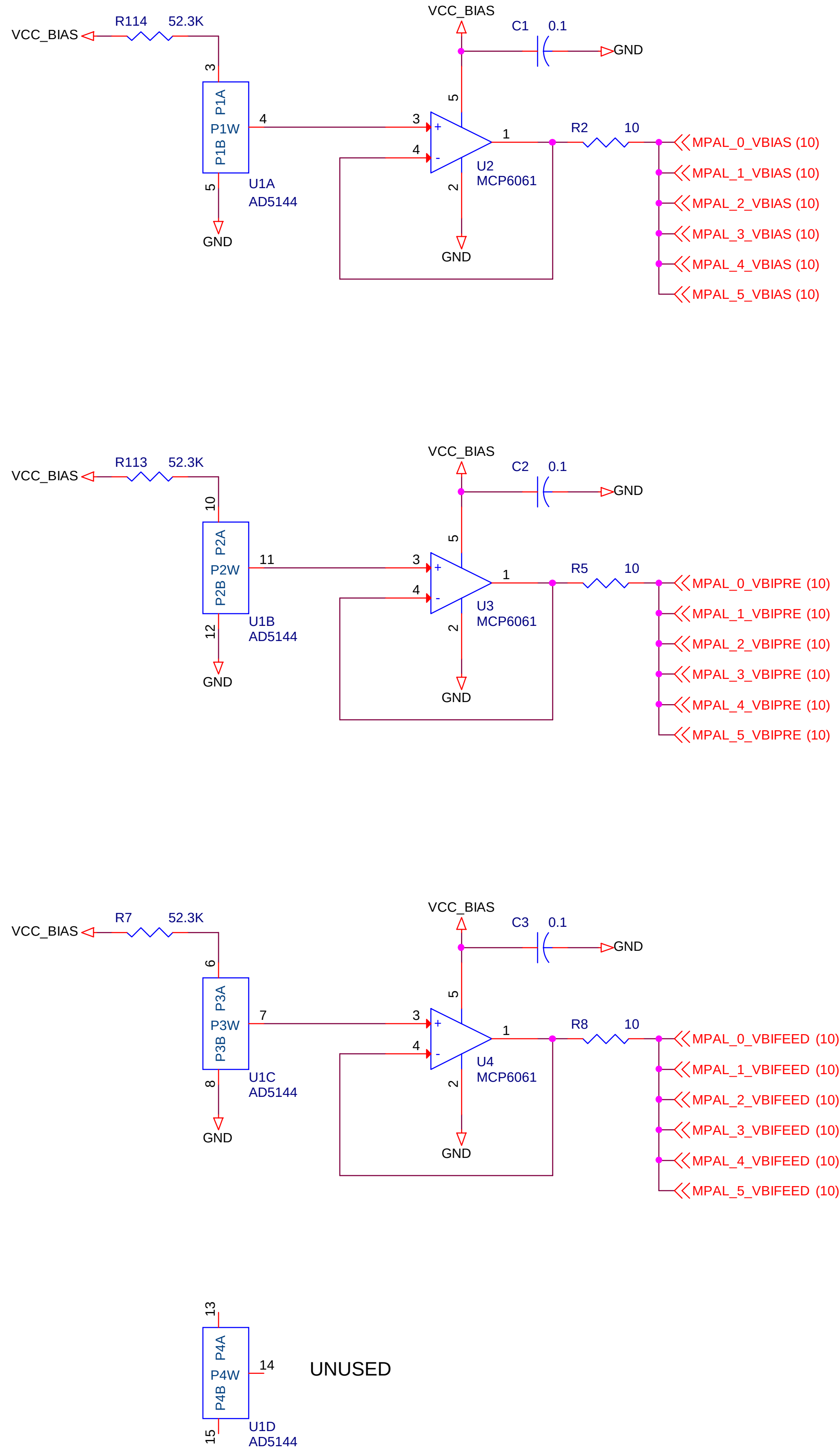
SHEET-11



THE OUTPUT RESISTOR IS INTENDED TO ISOLATE THE CAPACITIVE LOAD FROM THE OP-AMP, IF NECESSARY. IT CAN ALSO BE USED TO MEASURE THE BIAS CURRENTS.

THE DIGITAL POTS ARE NON-VOLATILE. THEY WILL BE WHERE THEY WERE LAST PROGRAMMED WHEN POWER IS APPLIED.

WITH A 52.5K SERIES RESISTOR AND 'VCC_BIAS' AT 2.5 VOLTS, THE OUTPUT VOLTAGE RANGE IS FROM 0.0 VOLTS TO 0.4 VOLTS. WITH 256 TAPS, THE STEP SIZE WILL BE 1.56 mV.

MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: BIAS VOLTAGE CONTROL

Size	Document Number	Rev
	<Doc>	V2

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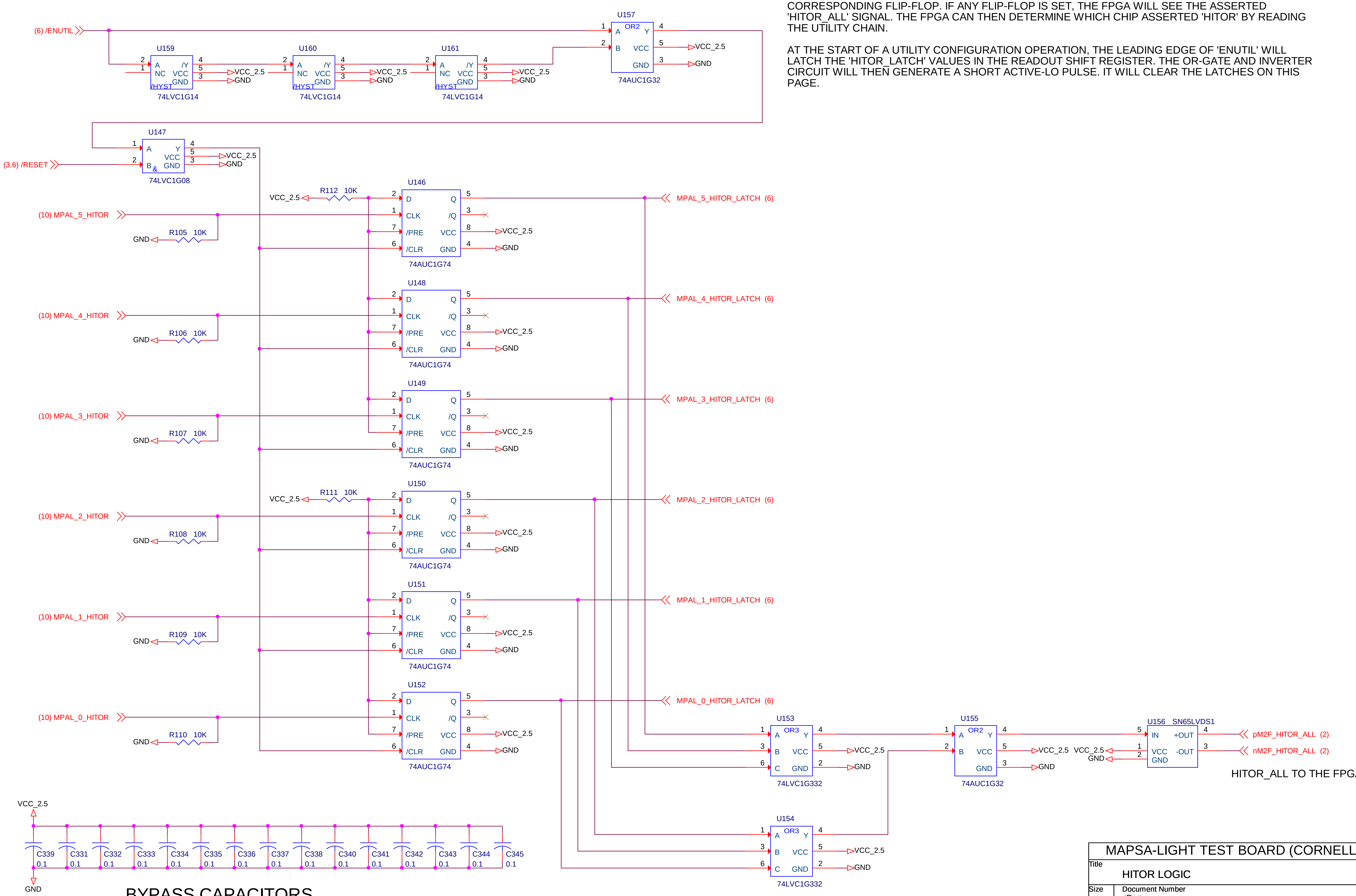
SHEET-12

A RISING EDGE ON A 'HITOR' SIGNAL FROM THE MAPSA-LIGHT WILL LATCH A '1' IN THE CORRESPONDING FLIP-FLOP. IF ANY FLIP-FLOP IS SET, THE FPGA WILL SEE THE ASSERTED 'HITOR_ALL' SIGNAL. THE FPGA CAN THEN DETERMINE WHICH CHIP ASSERTED 'HITOR' BY READING THE UTILITY CHAIN.

AT THE START OF A UTILITY CONFIGURATION OPERATION, THE LEADING EDGE OF 'ENUTIL' WILL LATCH THE 'HITOR_LATCH' VALUES IN THE READOUT SHIFT REGISTER. THE OR-GATE AND INVERTER CIRCUIT WILL THEN GENERATE A SHORT ACTIVE-LO PULSE. IT WILL CLEAR THE LATCHES ON THIS PAGE.



MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: HITOR LOGIC		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 12 of 12	