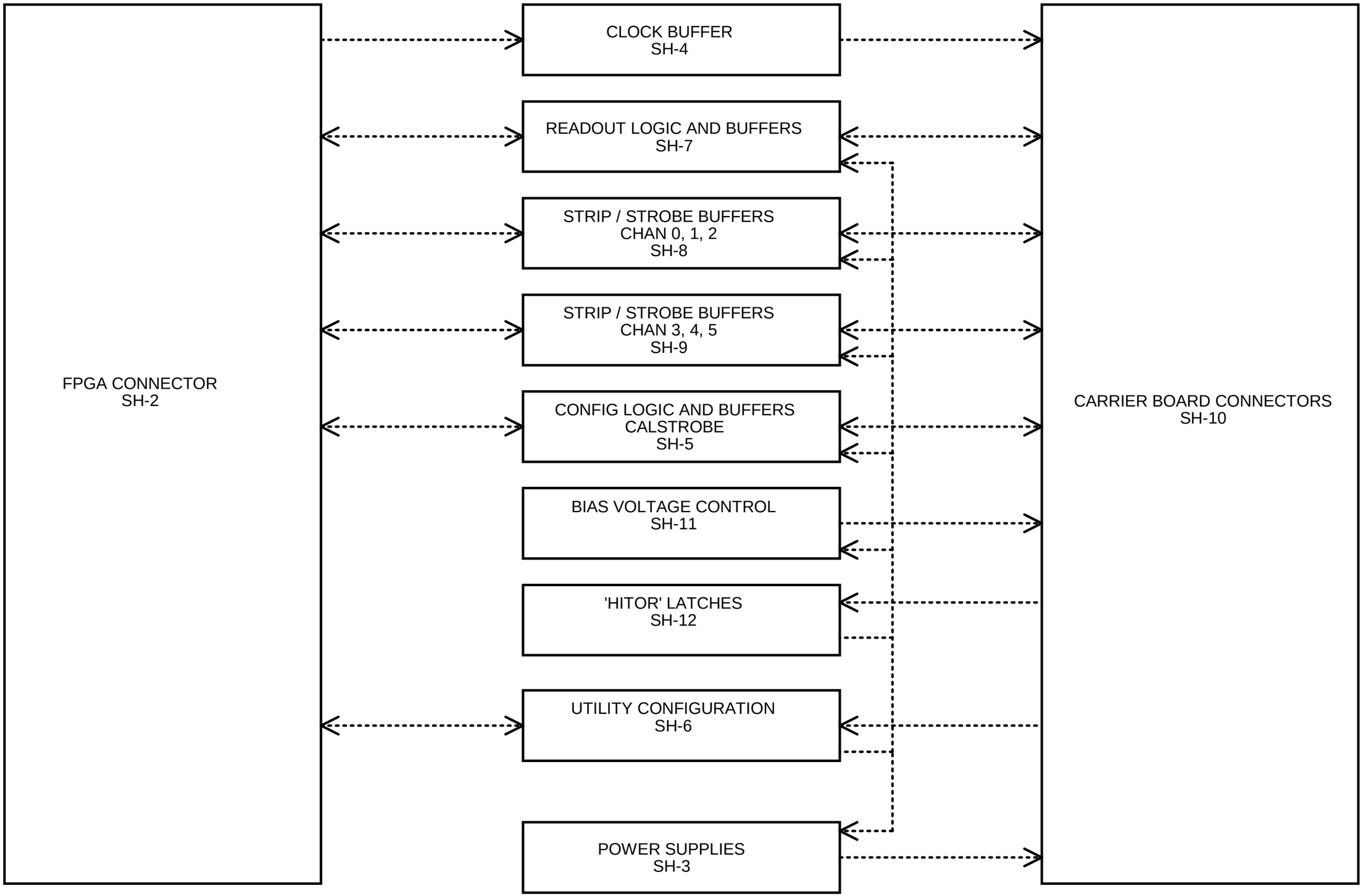


MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: BLOCK DIAGRAM

Size	Document Number	Rev
	<Doc>	V2

Date: Wednesday, June 17, 2015 Sheet 1 of 12

SHEET-2

J2B

LA00_P	G6	FPGA_CLK+ (4)
LA00_N	G7	FPGA_CLK- (4)
LA01_P	D8	F2M_0_PSTROBE (8)
LAO1_N	D9	F2M_0_NSTROBE (8)
LA02_P	H7	M2F_0_PSTROBE (8)
LA02_N	H8	M2F_0_NSTROBE (8)
LA03_P	G9	F2M_0_PSTRIP1 (8)
LA03_N	G10	F2M_0_NSTRIP1 (8)
LA04_P	H10	M2F_0_PSTRIP1 (8)
LA04_N	H11	M2F_0_NSTRIP1 (8)
LA05_P	D11	F2M_0_PSTRIP2 (8)
LA05_N	D12	F2M_0_NSTRIP2 (8)
LA06_P	C10	M2F_0_PSTRIP2 (8)
LA06_N	C11	M2F_0_NSTRIP2 (8)
LA07_P	H13	F2M_0_PSTRIP3 (8)
LA07_N	H14	F2M_0_NSTRIP3 (8)
LA08_P	G12	M2F_0_PSTRIP3 (8)
LA08_N	G13	M2F_0_NSTRIP3 (8)
LA09_P	D14	F2M_0_PSTRIP4 (8)
LA09_N	D15	F2M_0_NSTRIP4 (8)
LA10_P	C14	M2F_0_PSTRIP4 (8)
LA10_N	C15	M2F_0_NSTRIP4 (8)
LA11_P	H16	F2M_1_PSTROBE (8)
LA11_N	H17	F2M_1_NSTROBE (8)
LA12_P	G15	M2F_1_PSTROBE (8)
LA12_N	G16	M2F_1_NSTROBE (8)
LA13_P	D17	F2M_1_PSTRIP1 (8)
LA13_N	D18	F2M_1_NSTRIP1 (8)
LA14_P	C18	M2F_1_PSTRIP1 (8)
LA14_N	C19	M2F_1_NSTRIP1 (8)
LA15_P	H19	F2M_1_PSTRIP2 (8)
LA15_N	H20	F2M_1_NSTRIP2 (8)
LA16_P	G18	M2F_1_PSTRIP2 (8)
LA16_N	G19	M2F_1_NSTRIP2 (8)
LA17_P	D20	F2M_1_PSTRIP3 (8)
LA17_N	D21	F2M_1_NSTRIP3 (8)
LA18_P	C22	M2F_1_PSTRIP3 (8)
LA18_N	C23	M2F_1_NSTRIP3 (8)
LA19_P	H22	F2M_1_PSTRIP4 (8)
LA19_N	H23	F2M_1_NSTRIP4 (8)
LA20_P	G21	M2F_1_PSTRIP4 (8)
LA20_N	G22	M2F_1_NSTRIP4 (8)
LA21_P	H25	F2M_2_PSTROBE (8)
LA21_N	H26	F2M_2_NSTROBE (8)
LA22_P	G24	M2F_2_PSTROBE (8)
LA22_N	G25	M2F_2_NSTROBE (8)
LA23_P	D23	F2M_2_PSTRIP1 (8)
LA23_N	D24	F2M_2_NSTRIP1 (8)
LA24_P	H28	M2F_2_PSTRIP1 (8)
LA24_N	H29	M2F_2_NSTRIP1 (8)
LA25_P	G27	F2M_2_PSTRIP2 (8)
LA25_N	G28	F2M_2_NSTRIP2 (8)
LA26_P	D26	M2F_2_PSTRIP2 (8)
LA26_N	D27	M2F_2_NSTRIP2 (8)
LA27_P	C26	F2M_2_PSTRIP3 (8)
LA27_N	C27	F2M_2_NSTRIP3 (8)
LA28_P	H31	M2F_2_PSTRIP3 (8)
LA28_N	H32	M2F_2_NSTRIP3 (8)
LA29_P	G30	F2M_2_PSTRIP4 (8)
LA29_N	G31	F2M_2_NSTRIP4 (8)
LA30_P	H34	M2F_2_PSTRIP4 (8)
LA30_N	H35	M2F_2_NSTRIP4 (8)
LA31_P	G33	pM2F_OUTUTIL (6)
LA31_N	G34	nM2F_OUTUTIL (6)
LA32_P	H37	pF2M_DATAUTIL (6)
LA32_N	H38	nF2M_DATAUTIL (6)
LA33_P	G36	pF2M_CLKUTIL (6)
LA33_N	G37	nF2M_CLKUTIL (6)

CONN_GLIB_HPC

J2F

HA00_P	F4	F2M_3_PSTROBE (9)
HA00_N	F5	F2M_3_NSTROBE (9)
HA01_P	E2	M2F_3_PSTROBE (9)
HA01_N	E3	M2F_3_NSTROBE (9)
HA02_P	K7	F2M_3_PSTRIP1 (9)
HA02_N	K8	F2M_3_NSTRIP1 (9)
HA03_P	J6	M2F_3_PSTRIP1 (9)
HA03_N	J7	M2F_3_NSTRIP1 (9)
HA04_P	F7	F2M_3_PSTRIP2 (9)
HA04_N	F8	F2M_3_NSTRIP2 (9)
HA05_P	E6	M2F_3_PSTRIP2 (9)
HA05_N	E7	M2F_3_NSTRIP2 (9)
HA06_P	K10	F2M_3_PSTRIP3 (9)
HA06_N	K11	F2M_3_NSTRIP3 (9)
HA07_P	J9	M2F_3_PSTRIP3 (9)
HA07_N	J10	M2F_3_NSTRIP3 (9)
HA08_P	F10	F2M_3_PSTRIP4 (9)
HA08_N	F11	F2M_3_NSTRIP4 (9)
HA09_P	E9	M2F_3_PSTRIP4 (9)
HA09_N	E10	M2F_3_NSTRIP4 (9)
HA10_P	K13	F2M_4_PSTROBE (9)
HA10_N	K14	F2M_4_NSTROBE (9)
HA11_P	J12	M2F_4_PSTROBE (9)
HA11_N	J13	M2F_4_NSTROBE (9)
HA12_P	F13	F2M_4_PSTRIP1 (9)
HA12_N	F14	F2M_4_NSTRIP1 (9)
HA13_P	E12	M2F_4_PSTRIP1 (9)
HA13_N	E13	M2F_4_NSTRIP1 (9)
HA14_P	J15	F2M_4_PSTRIP2 (9)
HA14_N	J16	F2M_4_NSTRIP2 (9)
HA15_P	F16	M2F_4_PSTRIP2 (9)
HA15_N	F17	M2F_4_NSTRIP2 (9)
HA16_P	E15	F2M_4_PSTRIP3 (9)
HA16_N	E16	F2M_4_NSTRIP3 (9)
HA17_P	K16	M2F_4_PSTRIP3 (9)
HA17_N	K17	M2F_4_NSTRIP3 (9)
HA18_P	J18	F2M_4_PSTRIP4 (9)
HA18_N	J19	F2M_4_NSTRIP4 (9)
HA19_P	F19	M2F_4_PSTRIP4 (9)
HA19_N	F20	M2F_4_NSTRIP4 (9)
HA20_P	E18	pF2M_ENUTIL (6)
HA20_N	E19	nF2M_ENUTIL (6)
HA21_P	K19	pF2M_ENCONF (5)
HA21_N	K20	nF2M_ENCONF (5)
HA22_P	J21	pF2M_SHUTTER (7)
HA22_N	J22	nF2M_SHUTTER (7)
HA23_P	K22	pF2M_CALSTROBE (5)
HA23_N	K23	nF2M_CALSTROBE (5)

CONN_GLIB_HPC

J2G

HB00_P	K25	F2M_5_PSTROBE (9)
HB00_N	K26	F2M_5_NSTROBE (9)
HB01_P	J24	M2F_5_PSTROBE (9)
HB01_N	J25	M2F_5_NSTROBE (9)
HB02_P	F22	F2M_5_PSTRIP1 (9)
HB02_N	F23	F2M_5_NSTRIP1 (9)
HB03_P	E21	M2F_5_PSTRIP1 (9)
HB03_N	E22	M2F_5_NSTRIP1 (9)
HB04_P	F25	F2M_5_PSTRIP2 (9)
HB04_N	F26	F2M_5_NSTRIP2 (9)
HB05_P	E24	M2F_5_PSTRIP2 (9)
HB05_N	E25	M2F_5_NSTRIP2 (9)
HB06_P	K28	F2M_5_PSTRIP3 (9)
HB06_N	K29	F2M_5_NSTRIP3 (9)
HB07_P	J27	M2F_5_PSTRIP3 (9)
HB07_N	J28	M2F_5_NSTRIP3 (9)
HB08_P	F28	F2M_5_PSTRIP4 (9)
HB08_N	F29	F2M_5_NSTRIP4 (9)
HB09_P	E27	M2F_5_PSTRIP4 (9)
HB09_N	E28	M2F_5_NSTRIP4 (9)
HB10_P	K31	pM2F_0_OUTMEM (7)
HB10_N	K32	nM2F_0_OUTMEM (7)
HB11_P	J30	pM2F_1_OUTMEM (7)
HB11_N	J31	nM2F_1_OUTMEM (7)
HB12_P	F31	pM2F_2_OUTMEM (7)
HB12_N	F32	nM2F_2_OUTMEM (7)
HB13_P	E30	pM2F_3_OUTMEM (7)
HB13_N	E31	nM2F_3_OUTMEM (7)
HB14_P	K34	pM2F_4_OUTMEM (7)
HB14_N	K35	nM2F_4_OUTMEM (7)
HB15_P	J33	pM2F_5_OUTMEM (7)
HB15_N	J34	nM2F_5_OUTMEM (7)
HB16_P	F34	pF2M_CLKRO (7)
HB16_N	F35	nF2M_CLKRO (7)
HB17_P	K37	pF2M_DATARO (7)
HB17_N	K38	nF2M_DATARO (7)
HB18_P	J36	pM2F_OUTRO (7)
HB18_N	J37	nM2F_OUTRO (7)
HB19_P	E33	pF2M_CLKCONF (5)
HB19_N	E34	nF2M_CLKCONF (5)
HB20_P	F37	pF2M_DATACONF (5)
HB20_N	F38	nF2M_DATACONF (5)
HB21_P	E36	pM2F_OUTCONF (5)
HB21_N	E37	nM2F_OUTCONF (5)

CONN_GLIB_HPC

J2C

CONN_GLIB_HPC

DP0_C2M_P	C2	
DP0_C2M_N	C3	
DP0_M2C_P	C6	
DP0_M2C_N	C7	
DP1_C2M_P	A22	
DP1_C2M_N	A23	
DP1_M2C_P	A2	
DP1_M2C_N	A3	
DP2_C2M_P	A26	
DP2_C2M_N	A27	
DP2_M2C_P	A6	
DP2_M2C_N	A7	
DP3_C2M_P	A30	
DP3_C2M_N	A31	
DP3_M2C_P	A10	
DP3_M2C_N	A11	
GLIB_NC_DP4_C2M_P	A34	
GLIB_NC_DP4_C2M_N	A35	
GLIB_NC_DP4_M2C_P	A14	
GLIB_NC_DP4_M2C_N	A15	
GLIB_NC_DP5_C2M_P	A38	
GLIB_NC_DP5_C2M_N	A39	
GLIB_NC_DP5_M2C_P	A18	
GLIB_NC_DP5_M2C_N	A19	
GLIB_NC_DP6_C2M_P	B36	
GLIB_NC_DP6_C2M_N	B37	
GLIB_NC_DP6_M2C_P	B16	
GLIB_NC_DP6_M2C_N	B17	
GLIB_NC_DP7_C2M_P	B32	
GLIB_NC_DP7_C2M_N	B33	
GLIB_NC_DP7_M2C_P	B12	
GLIB_NC_DP7_M2C_N	B13	
GLIB_NC_DP8_C2M_P	B28	
GLIB_NC_DP8_C2M_N	B29	
GLIB_NC_DP8_M2C_P	B8	
GLIB_NC_DP8_M2C_N	B9	
GLIB_NC_DP9_C2M_P	B24	
GLIB_NC_DP9_C2M_N	B25	
GLIB_NC_DP9_M2C_P	B4	
GLIB_NC_DP9_M2C_N	B5	
GBT_CLK0_M2C_P	D4	
GBT_CLK0_M2C_N	D5	
GBT_CLK1_M2C_P	B20	
GBT_CLK1_M2C_N	B21	
CLK0_M2C_P	H4	
CLK0_M2C_N	H5	
CLK1_M2C_P	G2	pSPARE1
CLK1_M2C_N	G3	nSPARE1
CLK2_M2C_P	K4	pSPARE2
CLK2_M2C_N	K5	nSPARE2
CLK3_M2C_P	J2	pM2F_HITOR_ALL (12)
CLK3_M2C_N	J3	nM2F_HITOR_ALL (12)
PG_M2C	F1	
PG_C2M	D1	
PRSNT_M2C_L	H2	
VREF_A_M2C	H1	
VREF_B_M2C	K1	
RES0	B40	
RES1	B1	
TCK	D29	
TDI	D30	
TDO	D31	
TMS	D33	
TRST_L	D34	
GA1	D35	
GA0	C34	
SCL	C30	
SDA	C31	

J2A

CONN_GLIB_HPC

C35	C1	GND
C37	C4	GND
	C5	GND
	C8	GND
C39	C9	GND
D36	C12	GND
D38	C13	GND
D40	C16	GND
	C17	GND
	C20	GND
D32	C21	GND
	C24	GND
G39	C25	GND
H40	C28	GND
E39	C29	GND
F40	C32	GND
	C33	GND
K40	C36	GND
J39	C38	GND
	C40	GND
	D2	GND
	D3	GND
	D6	GND
	D7	GND
	D10	GND
	D13	GND
	D16	GND
	D19	GND
	D22	GND
	D25	GND
	D28	GND
	D37	GND
	D39	GND
	G1	GND
	G4	GND
	G5	GND
	G8	GND
	G11	GND
	G14	GND
	G17	GND
	G20	GND
	G23	GND
	G26	GND
	G29	GND
	G32	GND
	G35	GND
	G38	GND
	G40	GND
	H3	GND
	H6	GND
	H9	GND
	H12	GND
	H15	GND
	H18	GND
	H21	GND
	H24	GND
	H27	GND
	H30	GND
	H33	GND
	H36	GND
	H39	GND

+12.0V, +12.0V, +3.3V, +3.3V, +3.3V, +3.3V, +3.3VAUX, VADJ, VADJ, VADJ, VADJ, VIO_B_K40, VIO_B_J39

FPGA_PWR_OK (12)

J2D

CONN_GLIB_HPC

GND	A1	
GND	A4	
GND	A5	
GND	A8	
GND	A9	
GND	A12	
GND	A13	
GND	A16	
GND	A17	
GND	A20	
GND	A21	
GND	A24	
GND	A25	
GND	A28	
GND	A29	
GND	A32	
GND	A33	
GND	A36	
GND	A37	
GND	A40	
GND	B2	
GND	B3	
GND	B6	
GND	B7	
GND	B10	
GND	B11	
GND	B14	
GND	B15	
GND	B18	
GND	B19	
GND	B22	
GND	B23	
GND	B26	
GND	B27	
GND	B30	
GND	B31	
GND	B34	
GND	B35	
GND	B38	
GND	B39	
GND	E1	
GND	E4	
GND	E5	
GND	E8	
GND	E11	
GND	E14	
GND	E17	
GND	E20	
GND	E23	
GND	E26	
GND	E29	
GND	E32	
GND	E35	
GND	E38	
GND	E40	GND

J2E

CONN_GLIB_HPC

GND	F2	
GND	F3	
GND	F6	
GND	F9	
GND	F12	
GND	F15	
GND	F18	
GND	F21	
GND	F24	
GND	F27	
GND	F30	
GND	F33	
GND	F36	
GND	F39	
GND	J1	
GND	J4	
GND	J5	
GND	J8	
GND	J11	
GND	J14	
GND	J17	
GND	J20	
GND	J23	
GND	J26	
GND	J29	
GND	J32	
GND	J35	
GND	J38	
GND	J40	
GND	K2	
GND	K3	
GND	K6	
GND	K9	
GND	K12	
GND	K15	
GND	K18	
GND	K21	
GND	K24	
GND	K27	
GND	K30	
GND	K33	
GND	K36	
GND	K39	GND

NONE OF THE PIN ASSIGNMENTS HAVE BEEN OPTIMIZED!
NOT FOR ROUTING, AND NOT FOR PROPER BANK USAGE ON THE FPGA!

THE FOLLOWING ARE AVAILABLE AS GENERAL PURPOSE I/O: G2, G3, K4, K5, J2, J3.

CONNECTOR FOR 'VITA 57' HIGH PIN COUNT FMC. THIS MATES TO ONE OF THE FOLLOWING SAMTEC CABLES:
HDR-153514-01
HDR-153514-02
http://cloud.samtec.com/Prints/HDR-153514-XX-MKT.PDF
http://cloud.samtec.com/TestReports/hsc-report_HDR-153514-XX_Vita57-HPC_web.pdf

HOLE HT1, HOLE HT2 — HOLES FOR MOUNTING THE VITA-57 CONNECTOR

HOLE HT3, HOLE HT4 — HOLES FOR SUPPORTING THE BOARD.

MAPSA-LIGHT TEST BOARD (CORNELL U)

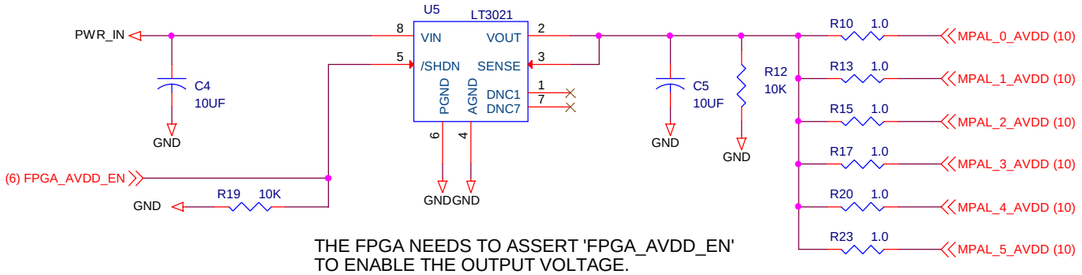
Title: FPGA CONNECTOR

Size | Document Number <Doc> | Rev V2

Date: Wednesday, June 17, 2015 | Sheet 2 of 12

SHEET-3

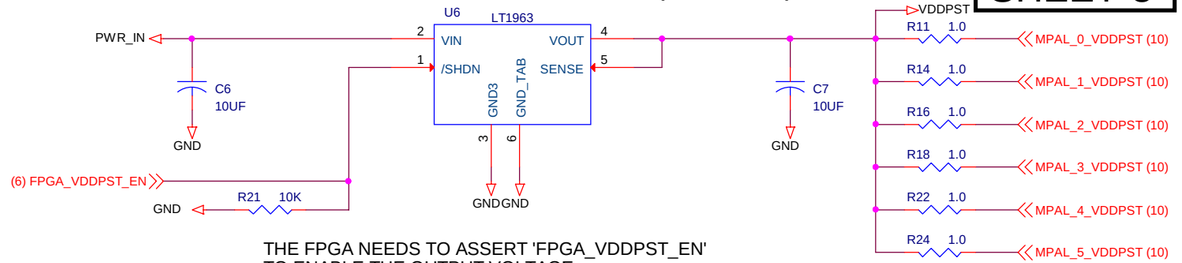
1.2 VOLT 500 MA ANALOG POWER SUPPLY (AVDD)



THE FPGA NEEDS TO ASSERT 'FPGA_AVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.

CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.

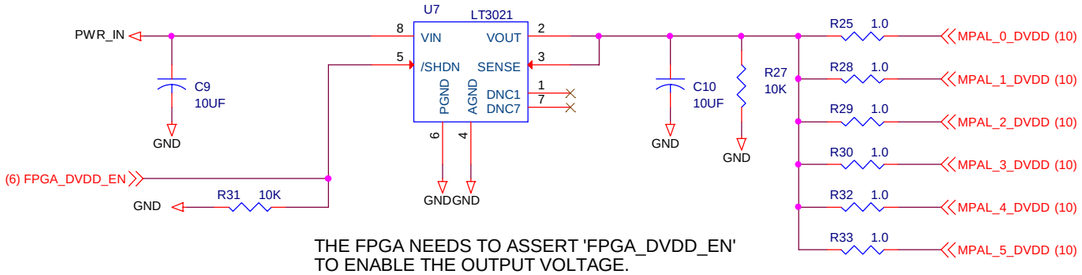
2.5 VOLT 1.5 A I/O POWER SUPPLY (VDDPST)



THE FPGA NEEDS TO ASSERT 'FPGA_VDDPST_EN' TO ENABLE THE OUTPUT VOLTAGE.

CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.

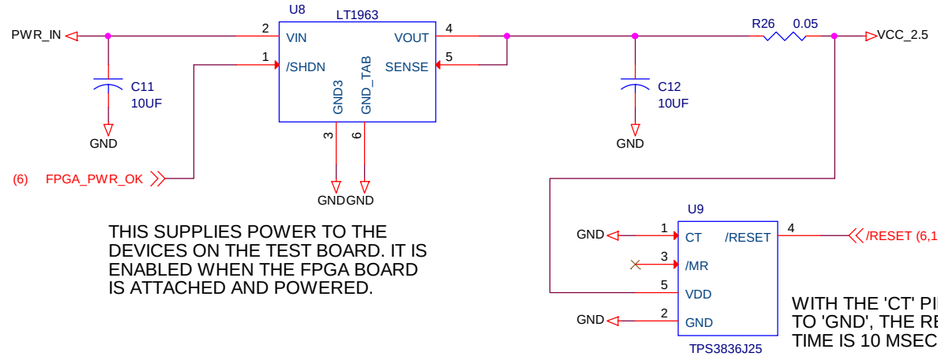
1.2 VOLT 500 MA DIGITAL POWER SUPPLY (DVDD)



THE FPGA NEEDS TO ASSERT 'FPGA_DVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.

CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.

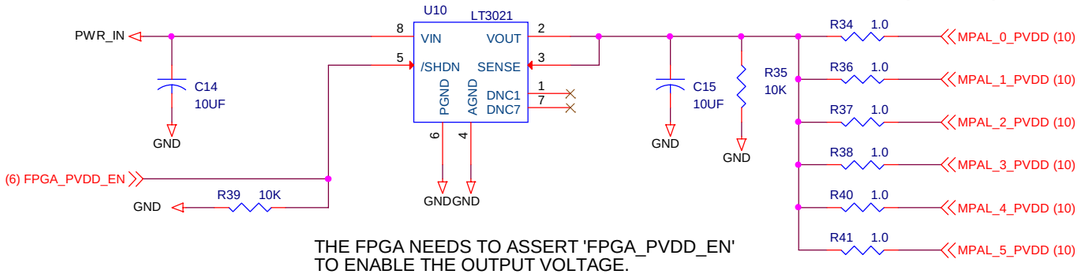
2.5 VOLT 1.5 A LOCAL POWER SUPPLY (VCC_2.5)



THIS SUPPLIES POWER TO THE DEVICES ON THE TEST BOARD. IT IS ENABLED WHEN THE FPGA BOARD IS ATTACHED AND POWERED.

WITH THE 'CT' PIN TIED TO 'GND', THE RESET TIME IS 10 MSEC.

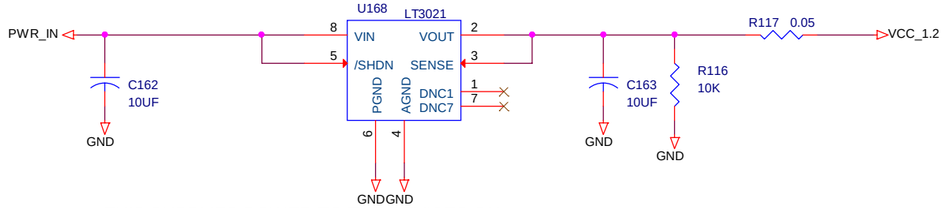
1.2 VOLT 500 MA PERIPHERY LOGIC POWER SUPPLY (PVDD)



THE FPGA NEEDS TO ASSERT 'FPGA_PVDD_EN' TO ENABLE THE OUTPUT VOLTAGE.

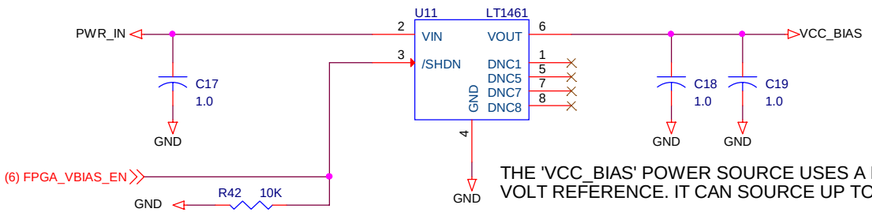
CURRENT FOR EACH READOUT CHIP CAN BE MEASURED.

1.2 VOLT 500 MA LOCAL POWER SUPPLY (VCC_1.2)



THIS SUPPLIES POWER TO THE DEVICES ON THE TEST BOARD. IT IS NOT SWITCHED.

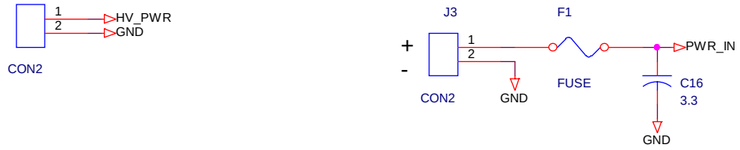
2.5 VOLT 50 MA BIAS VOLTAGE SOURCE (VCC_BIAS)



THE 'VCC_BIAS' POWER SOURCE USES A PRECISION 2.5 VOLT REFERENCE. IT CAN SOURCE UP TO 50 MA.

THE FPGA NEEDS TO ASSERT 'FPGA_BIAS_EN' TO ENABLE THE OUTPUT VOLTAGE.

HIGH VOLTAGE INPUT DC INPUT +3.3 TO +5



MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: POWER SUPPLIES		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 3 of 12	

THE INPUT IS CONFIGURED FOR 'LVDS'.
THE AC COUPLING CAPACITORS CAN BE REPLACED WITH ZERO-OHM JUMPERS IF AC COUPLING IS NOT DESIRED.

THE SY4016AR CHIP ACT AS LEVEL TRANSLATORS. THEIR INPUT SIGNAL IS AT 2.5 VOLTS. THEIR OUTPUT SIGNAL IS AT 1.2 VOLTS. THIS ALLOW DC COUPLING TO THE MAPSA-LIGHT CHIPS.

SHEET-4

(2) FPGA_CLK+
(2) FPGA_CLK-
R43 100
C20 0.1
C22 0.1

U12

14	CLKIN0	Q0	10
15	/CLKIN-	/Q0	9
19	CLKIN1	Q1	8
20	/CLKIN1	/Q1	7
17	VREF	Q2	5
23	CLK_SEL	/Q2	4
1	DIVA	Q3	43
33	DIVB	/Q3	42
3	SFOUTA0	Q4	41
GND	SFOUTA1	/Q4	40
31	SFOUTB0	Q5	38
GND	SFOUTB1	/Q5	37
16	OEA	Q6	36
18	OEB	/Q6	35
		Q7	30
		/Q7	29
		Q8	27
		/Q8	26
		Q9	25
		/Q9	24
		LOS0	13
		LOS1	21
		VDD	12 VCC_2.5
		VDDOA	44 VCC_2.5
		VDDOB	34 VCC_2.5
		GND	6 GND
		GND	22 GND
11	NC11	GND	39 GND
28	NC28	GND_PAD	45 GND

SI53302

INTERNAL BIAS RESISTORS KEEP UNUSED 'CLKIN' INPUTS AT SAFE LOGIC LEVELS.

THE 'CLK_SEL' PIN CONTAINS AN INTERNAL PULL-DOWN RESISTOR TO SELECT 'CLKIN0'.

FOR DIVIDE-BY-1 OUTPUTS, LEAVE THE 3-LEVEL 'DIVx' PINS OPEN.

FOR 'CML' OUTPUTS, CONNECT THE 3-LEVEL 'SFOUTx1' PINS TO 'GND' AND LEAVE THE 'SFOUTx0' PINS OPEN.

THE 'OEx' PINS CONTAINS AN INTERNAL PULL-UP RESISTOR TO ENABLE THE OUTPUTS.

THE 'LOSx' PINS ARE NOT USED IN THIS DESIGN.

PIN 45 IS THE "GND PAD" ON THE BOTTOM OF THE QFN PACKAGE.

U162 SY54016AR

2	IN	Q	7 MPAL_0_CLK+ (10)
3	/IN	/Q	6 MPAL_0_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

U163 SY54016AR

2	IN	Q	7 MPAL_1_CLK+ (10)
3	/IN	/Q	6 MPAL_1_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

U164 SY54016AR

2	IN	Q	7 MPAL_2_CLK+ (10)
3	/IN	/Q	6 MPAL_2_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

U165 SY54016AR

2	IN	Q	7 MPAL_3_CLK+ (10)
3	/IN	/Q	6 MPAL_3_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

U166 SY54016AR

2	IN	Q	7 MPAL_4_CLK+ (10)
3	/IN	/Q	6 MPAL_4_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

U167 SY54016AR

2	IN	Q	7 MPAL_5_CLK+ (10)
3	/IN	/Q	6 MPAL_5_CLK- (10)
		VCC	8 VCC_2.5
1	VT	VCCO	5 VCC_1.2
		GND	4 GND
		GND_PAD	9 GND

VCC_2.5
C267 0.1
C253 0.1
C254 0.1
C255 0.1
C256 0.1
C257 0.1
C258 0.1
C259 0.1
C260 0.1
GND

VCC_1.2
C273 0.1
C268 0.1
C269 0.1
C270 0.1
C271 0.1
C272 0.1
GND

BYPASS CAPACITORS

MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: CLOCK BUFFERS

Size	Document Number	Rev
	<Doc>	V2

Date: Wednesday, June 17, 2015 Sheet 4 of 12

SHEET-5

DATACONF FROM THE FPGA

(2) pF2M_DATACONF
(2) nF2M_DATACONF
U13 SN65LVDT2 (+IN, -IN, 110 OHM, OUT, VCC, GND) → VDDPST, GND

U203 74LVC1G14 (/Y, A, VCC, NC, GND, /HYST); VCC_2.5, GND

JP7 … JP12 JUMPER2

MPAL_0_OUTCONF (10)
MPAL_1_OUTCONF (10)
MPAL_2_OUTCONF (10)
MPAL_3_OUTCONF (10)
MPAL_4_OUTCONF (10)
MPAL_5_OUTCONF (10)

74AUC1G79 U197 … U202 (D, CLK, Q, VCC, GND)
R203 … R208 33

MPAL_0_DATACONF (10)
MPAL_1_DATACONF (10)
MPAL_2_DATACONF (10)
MPAL_3_DATACONF (10)
MPAL_4_DATACONF (10)
MPAL_5_DATACONF (10)

U26 SN65LVDS1 (IN, +OUT, -OUT, VCC, GND)
pM2F_OUTCONF (2)
nM2F_OUTCONF (2)

OUTCONF TO THE FPGA

(2) pF2M_CLKCONF
(2) nF2M_CLKCONF
U14 SN65LVDT2 (+IN, -IN, 110 OHM, OUT, VCC, GND) → VCC_2.5, GND

THIS BUFFER ACCEPTS A SINGLE 'CLKCONF' CONFIGURATION CLOCK FROM THE FPGA AND FANS IT OUT TO THE 6 MPA CHIPS.

U15 74ALVC244 (A1–A8, Y1–Y8, 1OE, 2OE, VCC, GND)
R44 … R49 33
MPAL_0_CLKCONF (10) … MPAL_5_CLKCONF (10)
R119 … R123 10K → GND

(2) pF2M_ENCONF
(2) nF2M_ENCONF
U18 SN65LVDT2 (+IN, -IN, 110 OHM, OUT, VCC, GND) → VCC_2.5, GND

THIS BUFFER ACCEPTS A SINGLE 'ENCONF' CONFIGURATION ENABLE SIGNAL FROM THE FPGA AND FANS IT OUT TO THE 6 MPA CHIPS.

U20 74ALVC244 (A1–A8, Y1–Y8, 1OE, 2OE, VCC, GND)
R50 … R55 33
MPAL_0_ENCONF (10) … MPAL_5_ENCONF (10)
R124 … R129 10K → GND

(2) pF2M_CALSTROBE
(2) nF2M_CALSTROBE
U23 SN65LVDT2 (+IN, -IN, 110 OHM, OUT, VCC, GND) → VCC_2.5, GND

THIS BUFFER ACCEPTS A SINGLE 'CALSTROBE' CALIBRATION STROBE SIGNAL FROM THE FPGA AND FANS IT OUT TO THE 6 MPA CHIPS.

U24 74ALVC244 (A1–A8, Y1–Y8, 1OE, 2OE, VCC, GND)
R56 … R61 33
MPAL_0_CALSTROBE (10) … MPAL_5_CALSTROBE (10)
R130 … R135 10K → GND

(7) /LOGIC_DRIVE_EN

THE '/LOGIC_DRIVE_EN' SIGNAL IS USED TO ENABLE SENDING DIGITAL SIGNAL LEVELS TO THE MAPSA-LIGHT INPUT PINS. IT IS POWERED FROM 'VDDPST'. THE OUTPUT WILL BE PULLED HIGH, TRI-STATING THE DRIVER CHIPS, UNTIL 'VDDPST' POWER APPEARS.

THE PULLDOWN RESISTORS KEEP THE MAPSA-LIGHT INPUTS AT A LOGIC ZERO UNTIL THE DRIVER IS ENABLED.

THE JUMPERS ON THE LEFT PROVIDE A BYPASS PATH FOR THE CONFIGURATION DATA STREAM. FOR NORMAL OPERATION, INSTALL JUMPERS FROM 1-TO-2 AND FROM 3-TO-4. TO BYPASS A CHANNEL, INSTALL A JUMPER FROM 1-TO-3 AND LEAVE 2-TO-4 OPEN.

THE FLIP-FLOPS ON THE RIGHT CONVERT THE SERIAL SHIFT-REGISTER CHAIN INTO AN 'SPI' CHAIN. THE FLIP-FLOPS WILL BE CLOCKED BY AN INVERTED COPY OF 'CLKCONF'.

THE FLIP-FLOPS ARE POWERED FROM 'VDDPST', WHICH IS THE SWITCHED SUPPLY THAT POWERS THE I/O LOGIC ON THE MAPSA CHIPS. THIS PREVENTS DRIVING ANY SIGNALS TO AN UNPOWERED MAPSA CHIP. THE SERIES RESISTORS PROVIDE SOURCE-SERIES TERMINATION.

VCC_2.5
C282 C274 C275 C276 C277 0.1
GND

VCC_2.5
C291 C283 C284 C285 C286 C287 C288 C289 C290 C293 0.1
GND

BYPASS CAPACITORS

MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: CONFIG LOGIC AND BUFFERS / CALSTROBE		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 5 of 12	

SHEET-6

U27 SN65LVDT2
(2) pF2M_DATAUTIL → 3 +IN; (2) nF2M_DATAUTIL → 4 -IN
110 OHM
OUT → 5
VCC → 1 → VCC_2.5
GND → 2 → GND

U28 SN65LVDT2
(2) pF2M_CLKUTIL → 3 +IN; (2) nF2M_CLKUTIL → 4 -IN
110 OHM
OUT → 5 → CLKUTIL
VCC → 1 → VCC_2.5
GND → 2 → GND

U190 74LVC1G14
CLKUTIL → 2 A
NC → 1
VCC → 4 → VCC_2.5
GND → 3 → GND
/Y → 5 → /CLKUTIL(12)
/HYST

U29 SN65LVDT2
(2) pF2M_ENUTIL → 3 +IN; (2) nF2M_ENUTIL → 4 -IN
110 OHM
OUT → 5 → ENUTIL
VCC → 1 → VCC_2.5
GND → 2 → GND

U30 74LVC1G14
ENUTIL → 2 A
NC → 1
VCC → 4 → VCC_2.5
GND → 3 → GND
/Y → 5 → /ENUTIL (12)
/HYST

THE 'ENUTIL' SIGNAL IS ACTIVE-HI. SOME UTILITY LOGIC REQUIRES AN ACTIVE-LOW SIGNAL.

THE AD5144 IN THE 20-PIN TSSOP PACKAGE DOES NOT HAVE A 'RESET' PIN NOR A 'DIS' PIN.

U1E AD5144
DATAUTIL → 19 SDI
CLKUTIL → 18 SCK
/ENUTIL → 1 /SYNC
SDO → 20
VLOG → 17 → VCC_2.5
VDD → 16 → VCC_2.5
VSS → 9 → GND
GND → 2 → GND
VCC_2.5 → R62 2.2K
VCC_2.5 → C46 3.3 → GND

BIAS VOLTAGE CONTROL

THE UTILITY CONFIGURATION BIT PATTERN IS 48-BITS LONG. IT CAN BE CLOCKED AT UP TO 50 MHZ.

THE 56-BIT FPGA REGISTER SHOULD BE CLOCKED OUT FROM THE 'MSB' AND CLOCKED INTO THE LSB.

U32 74LVC1G08
/ENUTIL → 1 A
(3,12) /RESET → 2 B
& → 4 Y → RCLK
VCC → 5 → VCC_2.5
GND → 3 → GND

U33 74LV595A
14 SER_IN; SER_OUT → 9
/CLKUTIL → 11 CLK
RCLK → 12 RCLK
GND → 13 /OE
(3,12) /RESET → 10 /CLR
QH → 7 → FPGA_DVDD_EN (3)
QG → 6 → FPGA_VDDPST_EN (3)
QF → 5 → SS_5_FROM_FPGA (9)
QE → 4 → SS_4_FROM_FPGA (9)
QD → 3 → SS_3_FROM_FPGA (9)
QC → 2 → SS_2_FROM_FPGA (8)
QB → 1 → SS_1_FROM_FPGA (8)
QA → 15 → SS_0_FROM_FPGA (8)
VCC → 16 → VCC_2.5
GND → 8 → GND

U34 74LV595A
14 SER_IN; SER_OUT → 9
/CLKUTIL → 11 CLK
RCLK → 12 RCLK
GND → 13 /OE
/CLR → 10
QH → 7
QG → 6
QF → 5
QE → 4
QD → 3
QC → 2 → FPGA_VBIAS_EN (3)
QB → 1 → FPGA_PVDD_EN (3)
QA → 15 → FPGA_AVDD_EN (3)
VCC → 16 → VCC_2.5
GND → 8 → GND

UTILITY DIGITAL OUTPUT

SERIAL DATA ARRIVES WITH 'MSB' FIRST. OUTPUT 'QH' IS THE 'MSB'.

DATA IS TRANSFERRED TO THE OUTPUT PINS ON THE TRAILING, RISING EDGE OF 'RCLK'. THIS IS DRIVEN BY THE TRAILING, RISING EDGE OF EITHER '/RESET' OR '/ENUTIL'.

ALL OUTPUT PINS WILL BE RESET TO ZERO AT POWER-UP.

U35 74LV165A
10 SER_IN; SER_OUT → 9
/CLKUTIL → 2 CLK; /SER_OUT → 7
GND → 15 CLK_INH
ENUTIL → 1 SH/LD
(12) MPAL_1_HITOR_LATCH → 6 H
(12) MPAL_0_HITOR_LATCH → 5 G
(10) MPAL_5_EMPTY → 4 F
(10) MPAL_4_EMPTY → 3 E
(10) MPAL_3_EMPTY → 14 D
(10) MPAL_2_EMPTY → 13 C
(10) MPAL_1_EMPTY → 12 B
(10) MPAL_0_EMPTY → 11 A
VCC → 16 → VCC_2.5
GND → 8 → GND

U36 74LV165A
10 SER_IN; SER_OUT → 9
/CLKUTIL → 2 CLK; /SER_OUT → 7
GND → 15 CLK_INH
ENUTIL → 1 SH/LD
(12) MPAL_5_HITOR_LATCH → 6 H
(12) MPAL_4_HITOR_LATCH → 5 G
(12) MPAL_3_HITOR_LATCH → 4 F
(12) MPAL_2_HITOR_LATCH → 3 E
14 D
13 C
12 B
11 A
VCC → 16 → VCC_2.5
GND → 8 → GND

U37 SN65LVDS1
5 IN; +OUT → 4 → pM2F_OUTUTIL (2)
VCC_2.5 → 1 VCC
GND → 2 GND
-OUT → 3 → nM2F_OUTUTIL (2)

UTILITY DIGITAL INPUT

SERIAL DATA LEAVES WITH 'MSB' FIRST. INPUT 'QH' IS THE 'MSB'.

DATA IS LATCHED IN THE INTERNAL SHIFT REGISTER ON THE RISING EDGE OF 'ENUTIL'. IT STREAMS OUT ON THE RISING EDGE OF 'CLKUTIL'.

VCC_2.5
C302 0.1; C294 0.1; C295 0.1; C296 0.1; C297 0.1; C298 0.1; C299 0.1; C300 0.1; C301 0.1; C303 0.1; C304 0.1; C305 0.1
GND

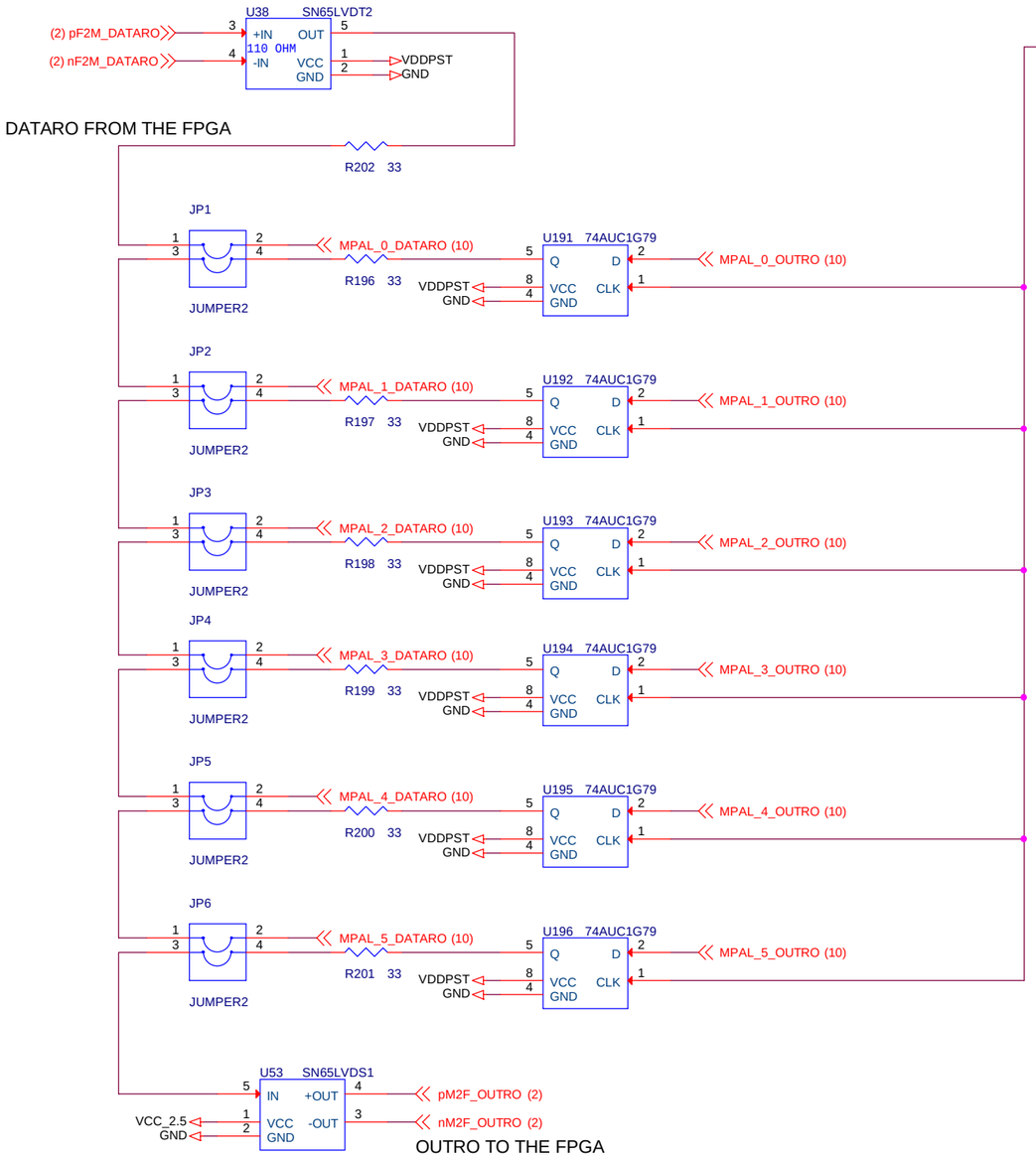
BYPASS CAPACITORS

UTILITY DIGITAL OUTPUT

UTILITY DIGITAL INPUT

MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: UTILITY CONFIGURATION		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 6 of 12	

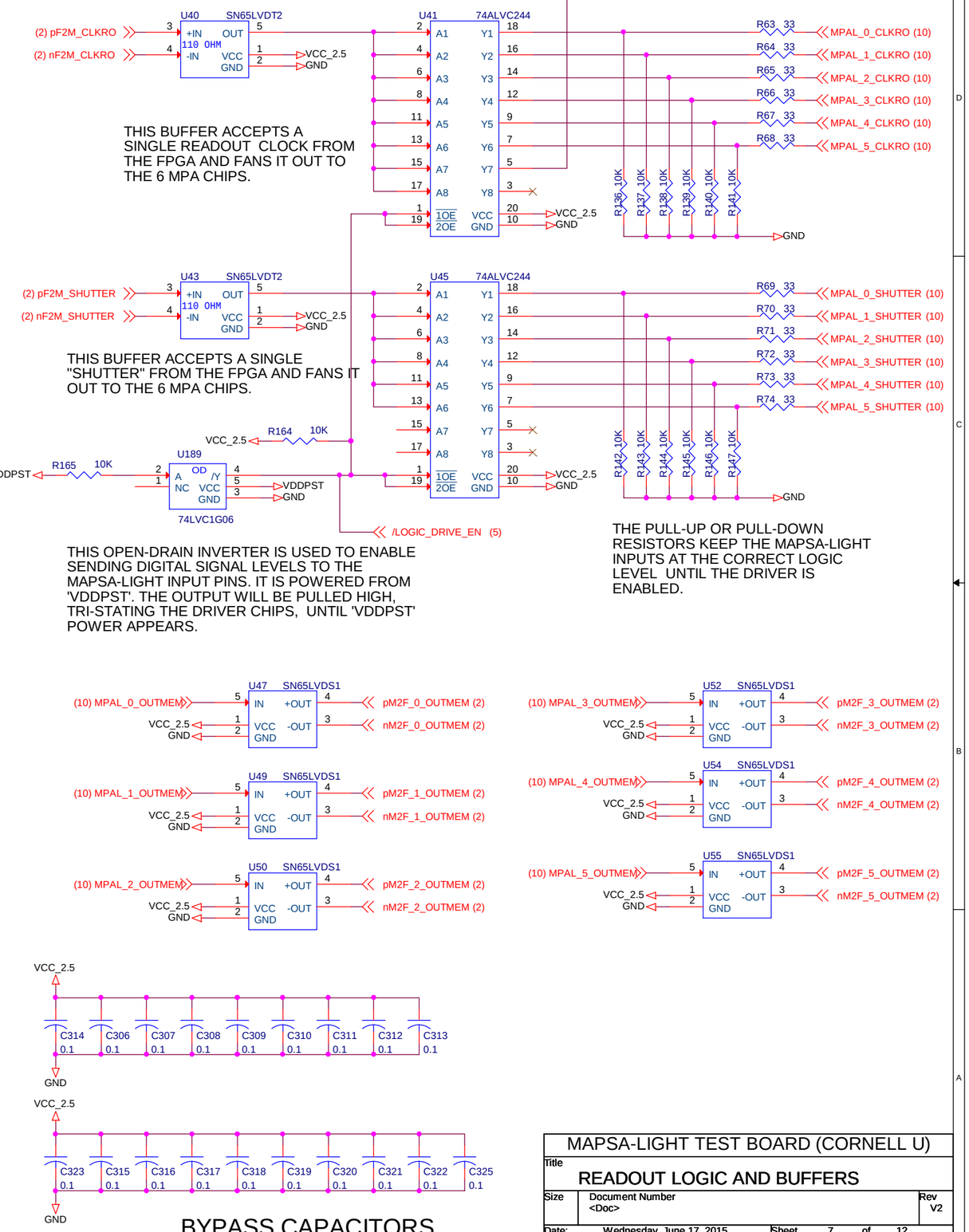
SHEET-7



THE JUMPERS ON THE LEFT PROVIDE A BYPASS PATH FOR THE READOUT DATA STREAM. FOR NORMAL OPERATION, INSTALL JUMPERS FROM 1-TO-2 AND FROM 3-TO-4. TO BYPASS A CHANNEL, INSTALL A JUMPER FROM 1-TO-3 AND LEAVE 2-TO-4 OPEN.

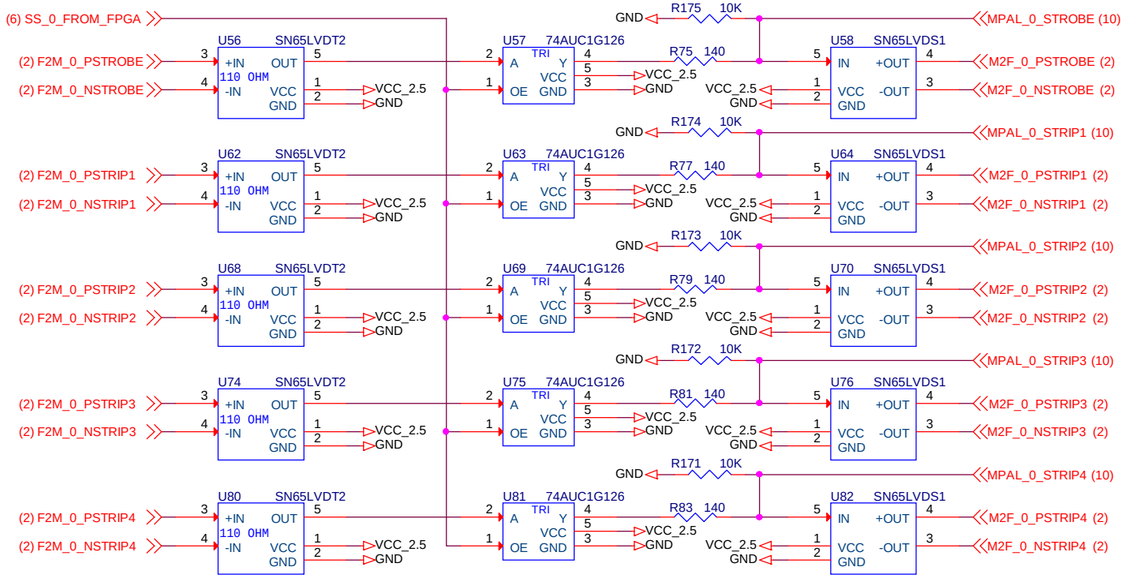
THE FLIP-FLOPS ON THE RIGHT CONVERT THE SERIAL SHIFT-REGISTER CHAIN INTO AN 'SPI' CHAIN. THE FLIP-FLOPS WILL BE CLOCKED BY A COPY OF 'CLKRO'. INVERSION IS NOT NEEDED, SINCE THE MAPSA CHIPS USE THE FALLING EDGE FOR THE READOUT SHIFT REGISTERS,

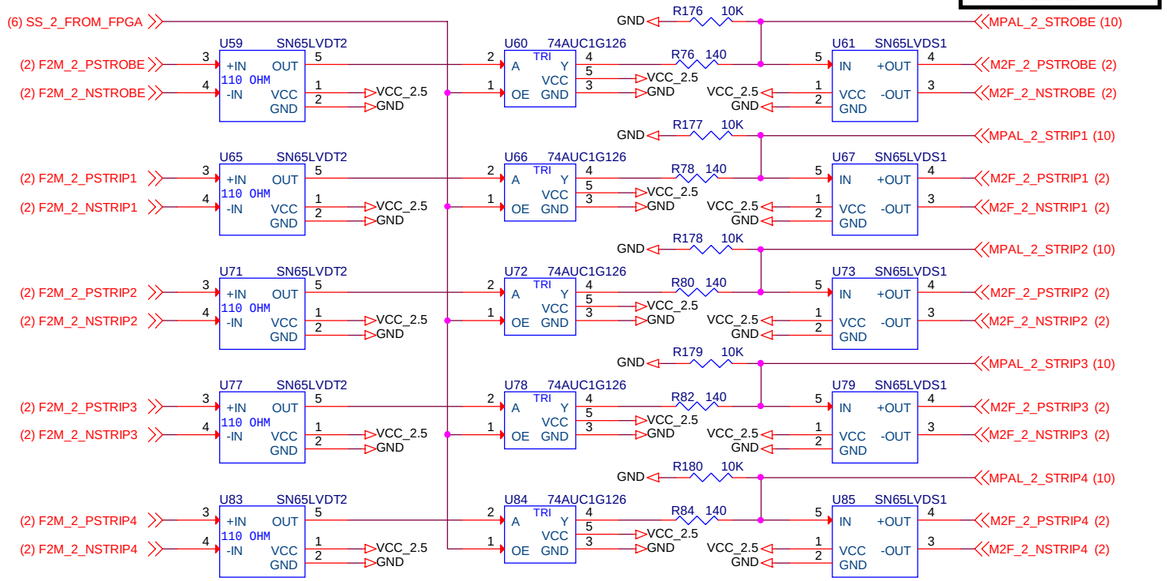
THE FLIP-FLOPS AND THE LVDS RECEIVER ARE POWERED FROM 'VDDPST', WHICH IS THE SWITCHED SUPPLY THAT POWERS THE I/O LOGIC ON THE MAPSA CHIPS. THIS PREVENTS DRIVING ANY SIGNALS TO AN UNPOWERED MAPSA CHIP. THE SERIES RESISTORS PROVIDE SOURCE-SERIES TERMINATION.

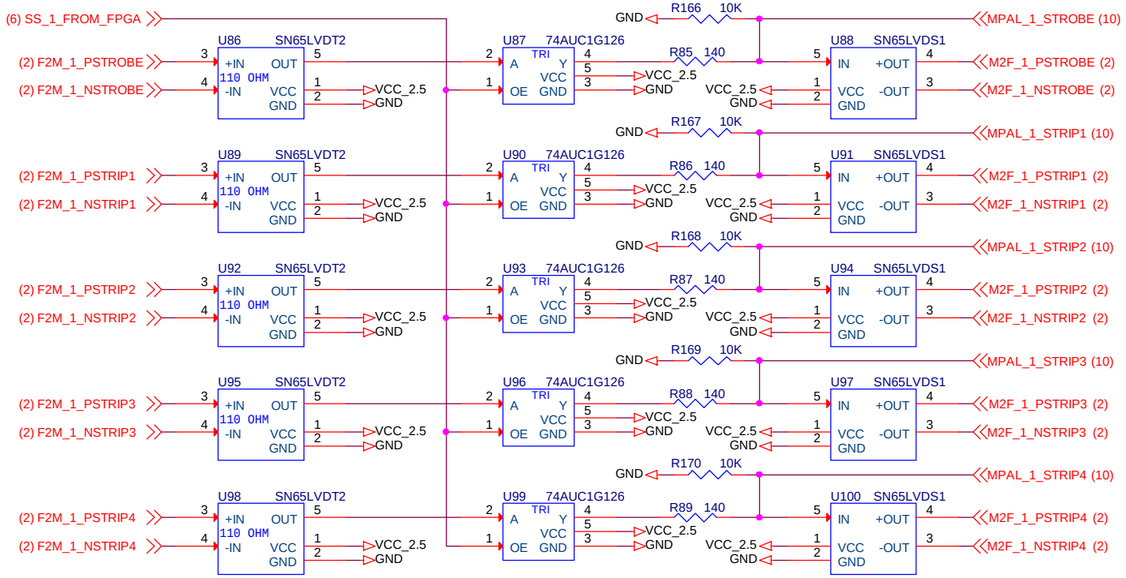


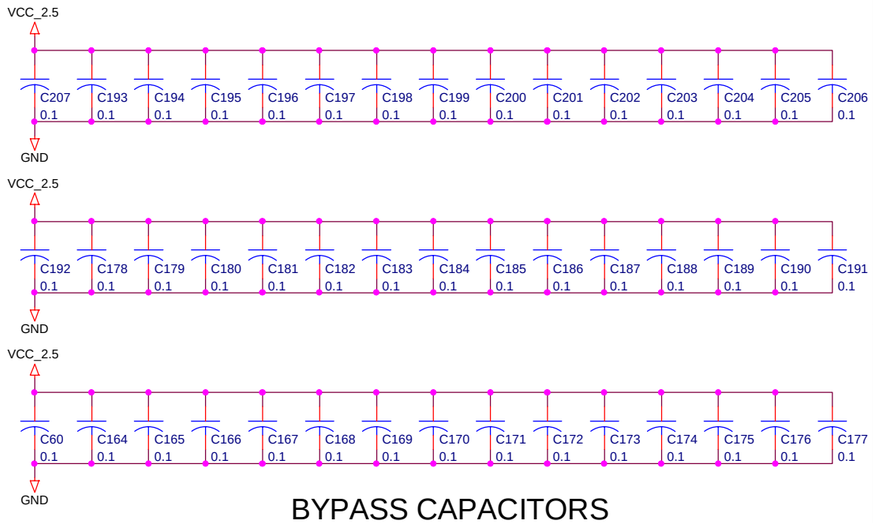
MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: READOUT LOGIC AND BUFFERS		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 7 of 12	

SHEET-8









BYPASS CAPACITORS

STRIP AND STROBE BUFFERING

ON THE MPA-LIGHT, STRIP AND STROBE ARE BI-DIRECTIONAL SIGNALS AT 160 MHZ. ON THE CABLE, THEY ARE UNI-DIRECTIONAL SIGNALS ON INDEPENDENT LVDS PAIRS.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE NEGATED (LOW) WHEN THE MPA-LIGHT CHIP IS SENDING DATA TO THE FPGA. THE BUFFER IS TRI-STATED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE ASSERTED (HIGH) WHEN THE MPA-LIGHT IS RECEIVING DATA FROM THE FPGA. THE BUFFER IS ENABLED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNALS WILL ALL BE NEGATED (LOW) AT POWER-UP. THE 10K PULL-DOWN RESISTORS WILL PROVIDE A LOGIC '0'.

THE 140 OHM RESISTOR LIMITS THE MAXIMUM CURRENT THAT CAN FLOW IF BOTH DRIVERS ARE INADVERTENTLY ACTIVE.

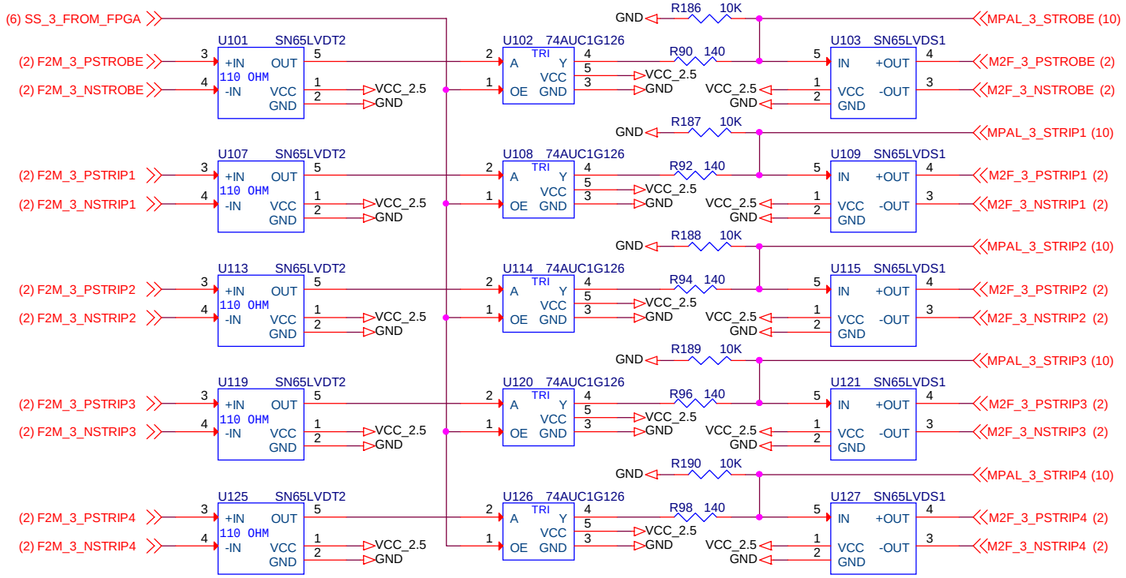
MAPSA-LIGHT TEST BOARD (CORNELL U)

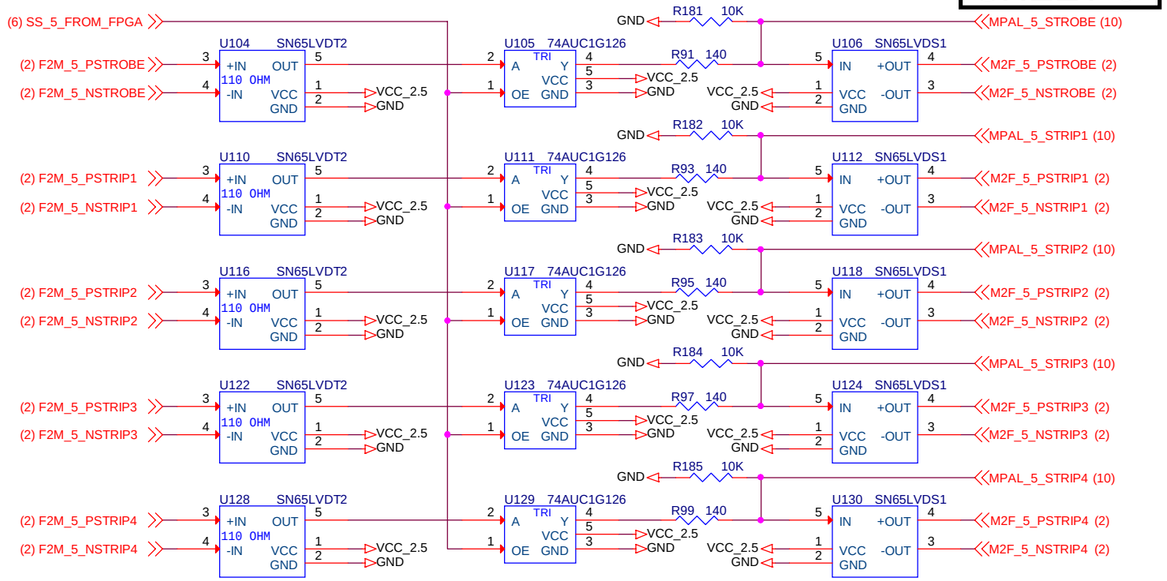
Title: STRIP / STROBE BUFFERS 0,1,2

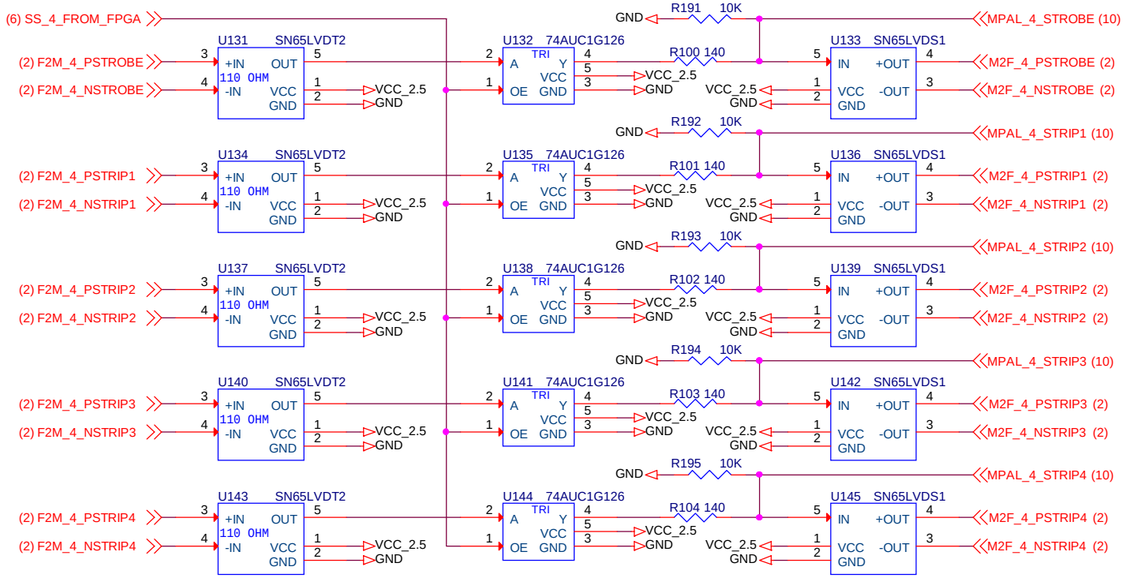
Size | Document Number: <Doc> | Rev: V2

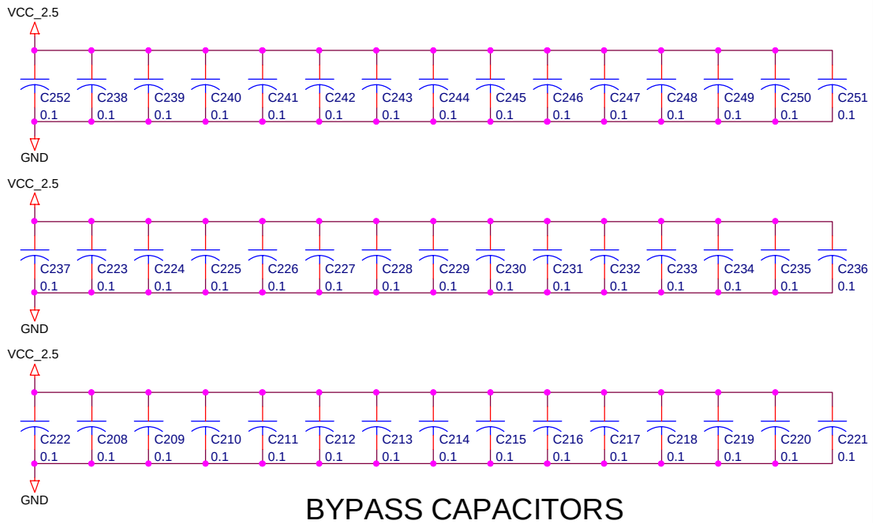
Date: Wednesday, June 17, 2015 | Sheet 8 of 12

SHEET-9









BYPASS CAPACITORS

STRIP AND STROBE BUFFERING

ON THE MPA-LIGHT, STRIP AND STROBE ARE BI-DIRECTIONAL SIGNALS AT 160 MHZ. ON THE CABLE, THEY ARE UNI-DIRECTIONAL SIGNALS ON INDEPENDENT LVDS PAIRS.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE NEGATED (LOW) WHEN THE MPA-LIGHT CHIP IS SENDING DATA TO THE FPGA. THE BUFFER IS TRI-STATED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNAL MUST BE ASSERTED (HIGH) WHEN THE MPA-LIGHT IS RECEIVING DATA FROM THE FPGA. THE BUFFER IS ENABLED IN THIS CONDITION.

THE 'SS_x_FROM_FPGA' SIGNALS WILL ALL BE NEGATED (LOW) AT POWER-UP. THE 10K PULL-DOWN RESISTORS WILL PROVIDE A LOGIC '0'.

THE 140 OHM RESISTOR LIMITS THE MAXIMUM CURRENT THAT CAN FLOW IF BOTH DRIVERS ARE INADVERTENTLY ACTIVE.

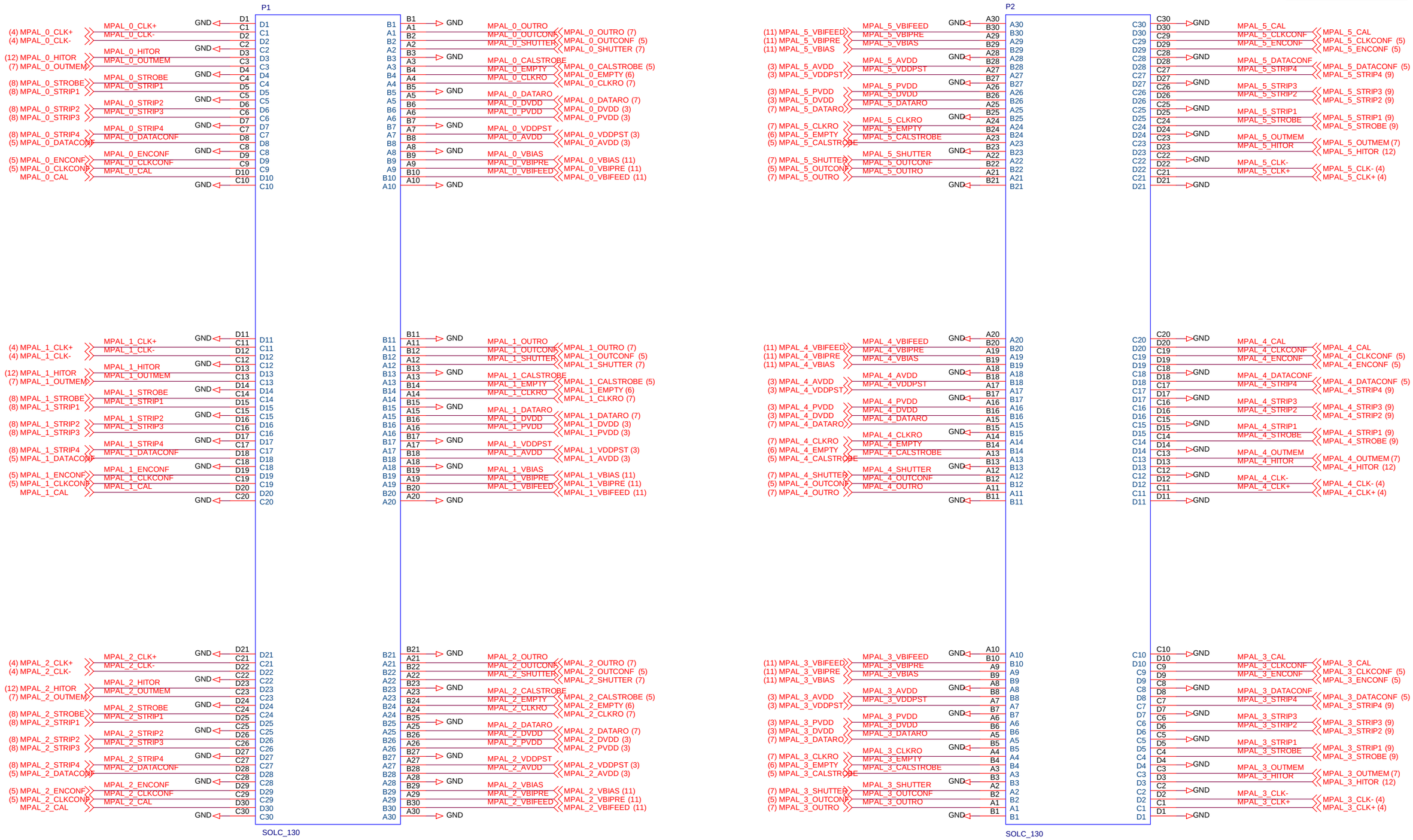
MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: STRIP / STROBE BUFFERS 3,4,5

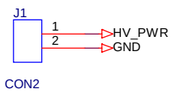
Size | Document Number: <Doc> | Rev: V2

Date: Wednesday, June 17, 2015 | Sheet 9 of 12

SHEET-10

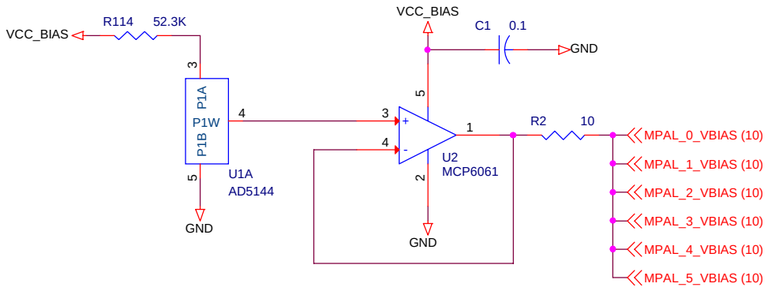


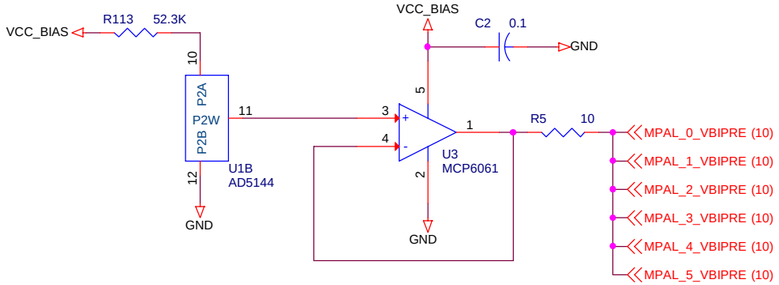
HIGH VOLTAGE OUTPUT

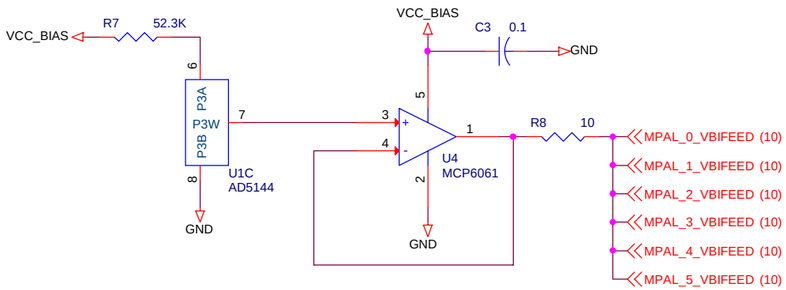


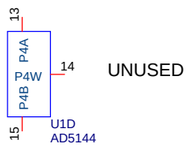
MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: CARRIER BOARD CONNECTORS		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 10 of 12	

SHEET-11









UNUSED

THE OUTPUT RESISTOR IS INTENDED TO ISOLATE THE CAPACITIVE LOAD FROM THE OP-AMP, IF NECESSARY. IT CAN ALSO BE USED TO MEASURE THE BIAS CURRENTS.

THE DIGITAL POTS ARE NON-VOLATILE. THEY WILL BE WHERE THEY WERE LAST PROGRAMMED WHEN POWER IS APPLIED.

WITH A 52.5K SERIES RESISTOR AND 'VCC_BIAS' AT 2.5 VOLTS, THE OUTPUT VOLTAGE RANGE IS FROM 0.0 VOLTS TO 0.4 VOLTS. WITH 256 TAPS, THE STEP SIZE WILL BE 1.56 mV.

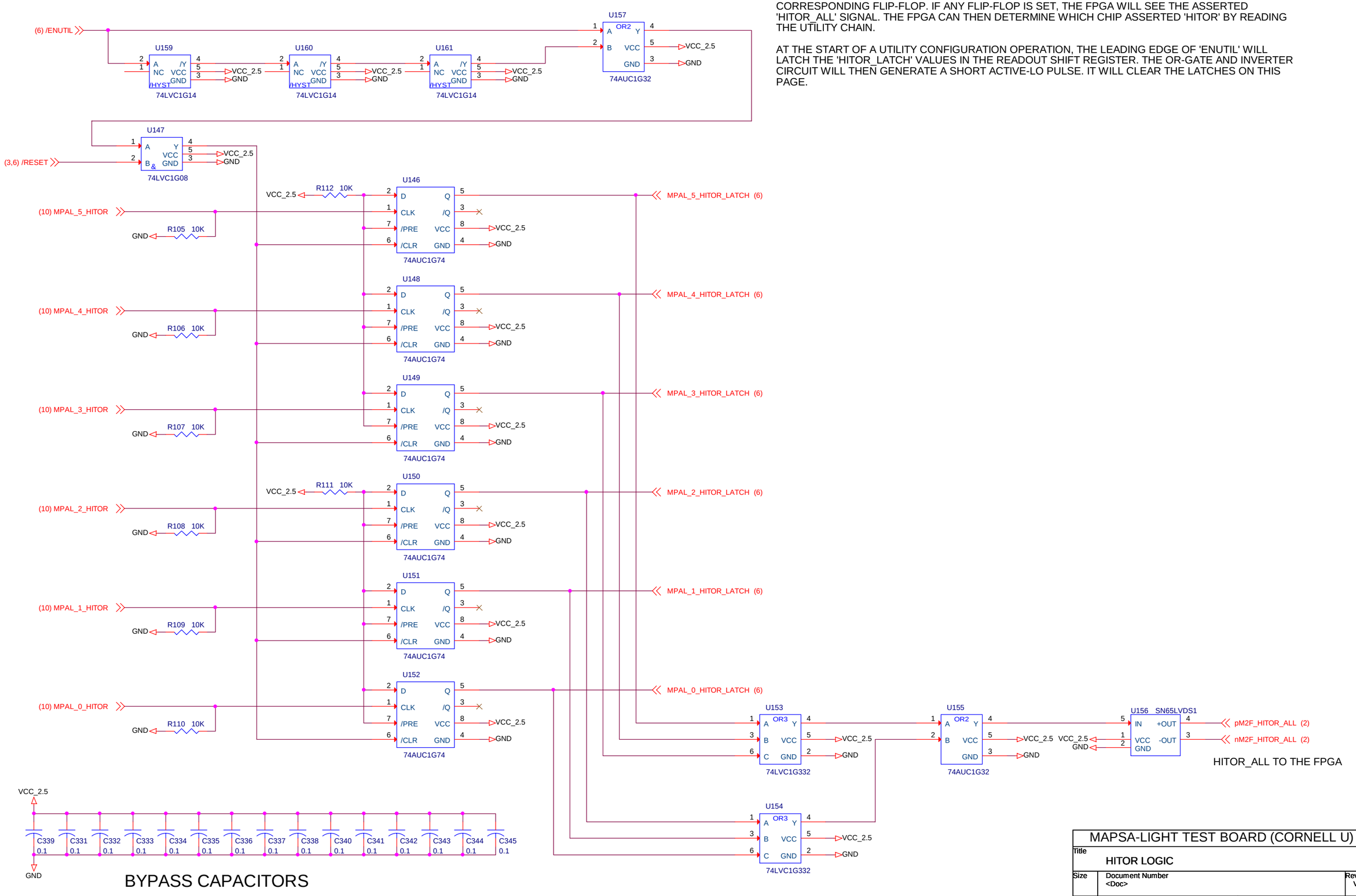
MAPSA-LIGHT TEST BOARD (CORNELL U)

Title: BIAS VOLTAGE CONTROL		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 11 of 12	

SHEET-12

A RISING EDGE ON A 'HITOR' SIGNAL FROM THE MAPSA-LIGHT WILL LATCH A '1' IN THE CORRESPONDING FLIP-FLOP. IF ANY FLIP-FLOP IS SET, THE FPGA WILL SEE THE ASSERTED 'HITOR_ALL' SIGNAL. THE FPGA CAN THEN DETERMINE WHICH CHIP ASSERTED 'HITOR' BY READING THE UTILITY CHAIN.

AT THE START OF A UTILITY CONFIGURATION OPERATION, THE LEADING EDGE OF 'ENUTIL' WILL LATCH THE 'HITOR_LATCH' VALUES IN THE READOUT SHIFT REGISTER. THE OR-GATE AND INVERTER CIRCUIT WILL THEN GENERATE A SHORT ACTIVE-LO PULSE. IT WILL CLEAR THE LATCHES ON THIS PAGE.



MAPSA-LIGHT TEST BOARD (CORNELL U)		
Title: HITOR LOGIC		
Size	Document Number <Doc>	Rev V2
Date: Wednesday, June 17, 2015	Sheet 12 of 12	