SP605 Reference Design User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
11/09/2009	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This user guide introduces several designs that demonstrate Spartan®-6 FPGA features using the SP605 evaluation board.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "SP605 Evaluation Board," provides an overview of the Spartan-6 FPGA, components and features of the SP605 board, and supporting reference designs.
- Appendix A, "References."

Additional Documentation

The following documents are available for download at http://www.xilinx.com/products/spartan6/

- Spartan®-6 Datasheet: Family Overview

  The features and products of the Spartan®-6 family are outlined in this overview.
- Spartan®-6 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Spartan®-6 family.
- Spartan®-6 FPGA Packaging and Pinouts User Guide

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- Spartan®-6 FPGA Configuration User Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (Serial, SelectMAP, and Master BPI), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- Spartan®-6 FPGA Select I/O Resources User Guide

  This user guide details input/output characteristics and SelectIO™ logic resources available in Spartan®-6 FPGAs.
- Spartan®-6 FPGA Clocking Resources User Guide

  This document describes Spartan®-6 FPGA clocking.
- Spartan®-6 FPGA Block RAM Resources User Guide

This guide describes the Spartan®-6 FPGA block RAMs. Block RAMs are used for efficient data storage or buffering, for high-performance state machines or FIFO buffer, for large shift registers, large look-up tables, or ROMs.

- Spartan®-6 FPGA Configurable Logic Block User Guide

  This guide describes the Spartan®-6 FPGA configurable logic blocks (CLBs). Including the varying capabilities of the look-up tables (LUTs), the physical direction of the carry propagation, the number and distribution of the available flip-flops, and the availability of the very efficient shift registers.

- Spartan®-6 FPGA GTP Transceivers User Guide

  This document shows how to use the GTP transceivers in Spartan®-6 FPGAs.

- Spartan®-6 FPGA Memory Controller User Guide

  This document describes the Spartan®-6 FPGA memory controller.

- Spartan®-6 FPGA DSP48A1 Slice User Guide

  This user guide is a detailed functional description of the DSP48A1 slice in Spartan®-6 FPGAs. The Spartan®-6 family offers a high ratio of DSP48A1 slices to logic, making it ideal for math-intensive applications. Refer to the Spartan®-6 Family Overview for the number of DSP48A1 slices for each Spartan®-6 device.

- Spartan®-6 FPGA Hardware User Guide

  Chapters in this manual cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- LogiCORE Datasheet: Multi-port Memory Controller (MPMC)

  This datasheet details the use of the MPMC compatible with the Spartan®-6 FPGAs.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

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Chapter 1

SP605 Evaluation Board

Introduction

The Spartan®-6 family [Ref 1] provides leading system integration capabilities with the lowest total cost for high-volume applications. The thirteen-member family delivers expanded densities ranging from 3,400 to 148,000 logic cells, with half the power consumption of previous Spartan families and faster, more comprehensive connectivity. Built on a mature 45 nm low-power copper process technology that delivers the optimal balance of cost, power, and performance, the Spartan®-6 family offers a new, more efficient, dual-register 6-input look-up table (LUT) logic and a rich selection of built-in system-level blocks. These include 18 Kb block RAMs, second generation DSP48A1 slices, SDRAM memory controllers, enhanced mixed-mode clock management blocks, SelectIO™ technology, power-optimized high-speed serial transceiver blocks, PCI Express™ compatible Endpoint blocks, advanced system-level power management modes, autodetect configuration options, and enhanced IP security with AES and Device DNA protection. These features provide a low-cost programmable alternative to custom ASIC products with unprecedented ease-of-use. Spartan®-6 FPGAs are the programmable silicon foundation for Targeted Design Platforms that deliver integrated software and hardware components to enable designers to focus on innovation as soon as their development cycle begins.

The SP605 Evaluation Kit is based on the XC6SLX45T-3FGG484 Spartan-6 FPGA. This FPGA contains 43,661 logic cells, a rating that reflects the increased logic capacity offered by the new six-input LUT architecture. For additional information, see the *Spartan-6 Family FPGAs Product Table* at http://www.xilinx.com/publications/prod_mktg/Spartan6_Product_Table.pdf.

The Built-In Self Test (BIST), feature demonstrations, and reference design files are provided with the SP605 Evaluation Kit. The CompactFlash card included with the kit contains a BIST application. The BIST provides a convenient way to test many of the board's features on power-up and upon reconfiguration through the System ACE CF JTAG interface. After running through the tutorial provided in *Getting Started with the Xilinx Spartan-6 FPGA SP605 Evaluation Kit*, the tutorials and reference designs available on the SP605 Web page can be used to further explore the capabilities of the SP605 and the Spartan-6 FPGA.

For the most up-to-date information on the tutorial content provided with the SP605 Evaluation Kit, see the SP605 Reference Design Web page at http://www.xilinx.com/products/boards/sp605/reference_designs.htm.

SP605 Features

The SP605 designs demonstrate Spartan-6 FPGA features using the SP605 evaluation board. These features include:

- 128 MB DDR3 Component
- 8 MB SPI x4 Flash and headers
- 32 MB Linear BPI Flash
- System ACE CF
- USB JTAG
- Video VGA
- 10/100/1000 Tri-Speed Ethernet PHY
- GTP port with SMA x4
- 200 MHz differential clock, 27 MHz socketed oscillator, clock SMA connectors
- MGT clocking SMA x2
- SFP module connector
- VITA 57.1 FMC LPC connector
- PCIe® Gen1 (1-lane)
- UART (via USB cable)
- IIC EEPROM
- LEDs
- DIP Switch
- Pushbuttons
- Power Monitoring
- Power supply: 12V AC Adapter or 12V 4-pin ATX

For detailed information on the features of the SP605 board, see the *SP605 Hardware User Guide*. [Ref 3]

Reference Designs

Built-In Self Test (BIST)

The BIST tests the operation of many of the SP605 Evaluation Kit features. When configured to boot from the CompactFlash memory, the BIST menu appears upon power-up. After FPGA configuration, the text shown in Figure 1-1 appears in a terminal program window, such as Tera Term. Type the number associated with one of the listed tests to run the test application. For example, typing a "5" runs the IIC Test application.

See the SP605 *Built-In Self Test Flash Application* tutorial for more information on the BIST software and its operation. [Ref 18]

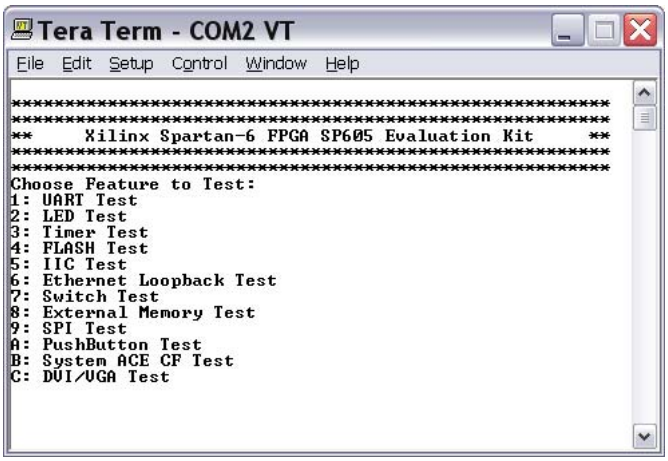

Figure 1-1: **BIST Initial Screen**

The default location of the BIST program is at System ACE CF configuration address 0 on the CompactFlash (CF) card included with the SP605 Evaluation Kit. The *SP605 Restoring Flash Contents* tutorial provides instructions for restoring the image to its factory default content. [Ref 24]

MIG DDR3 Design

The Spartan-6 FPGA contains dedicated Memory Controller Blocks (MCB) for simplified DRAM interfaces, including up to four MCB cores in a single Spartan-6 device. The FPGA also contains an embedded controller and physical (PHY) interface, 4-bit, 8-bit, or 16-bit single component memory support, and memory densities up to 4 Gb. Additionally, the Spartan-6 FPGA is capable of performance up to 800 Mb/s (400 MHz double data rate).

For the logic designer, the Memory Interface Generator (MIG) tool (Figure 1-2) can be use to create a simple user interface that abstracts away the complexity of memory transactions. The integrated memory controller block's assembly and signal connectivity is made transparent to the user.

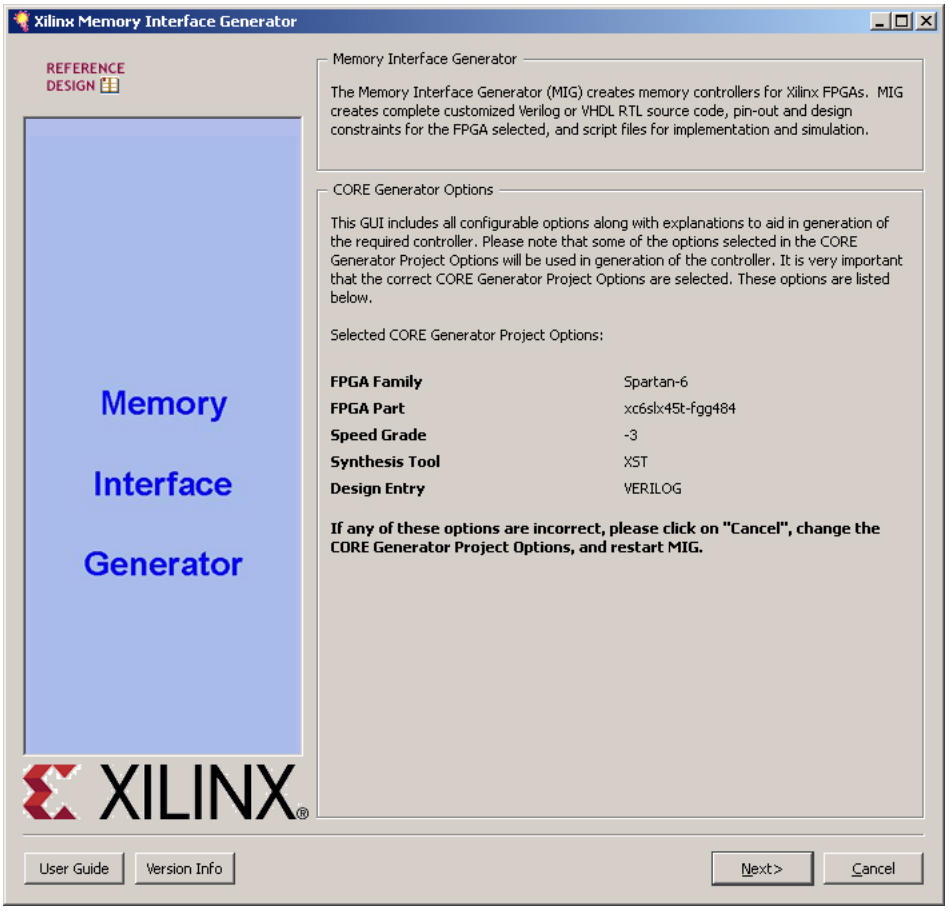

Figure 1-2: **MIG Graphical User Interface**

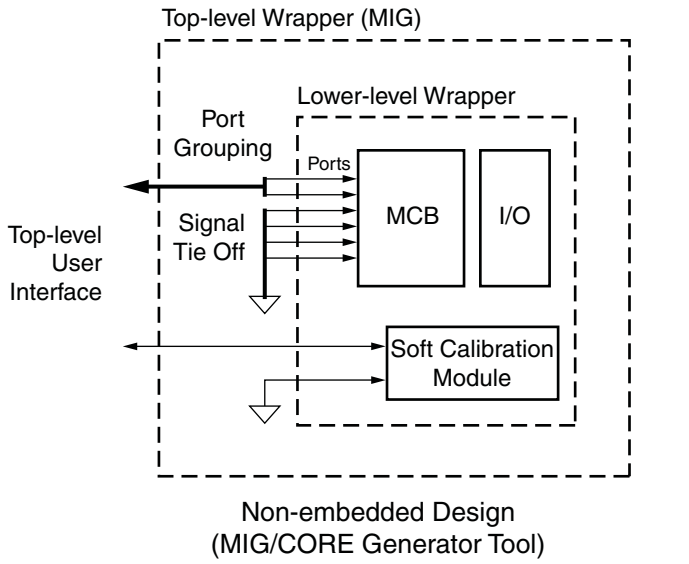

Figure 1-3: **MIG Wrapper for Non-embedded Design**

The LogiCORE™ MIG example debug design tests the DDR3 memory interface through a series of writes and reads with pattern verification. The example design was generated using the option to include the debug interface. The results can be viewed in the ChipScope Pro Analyzer tool as shown in Figure 1-4, page 11. [Ref 19]

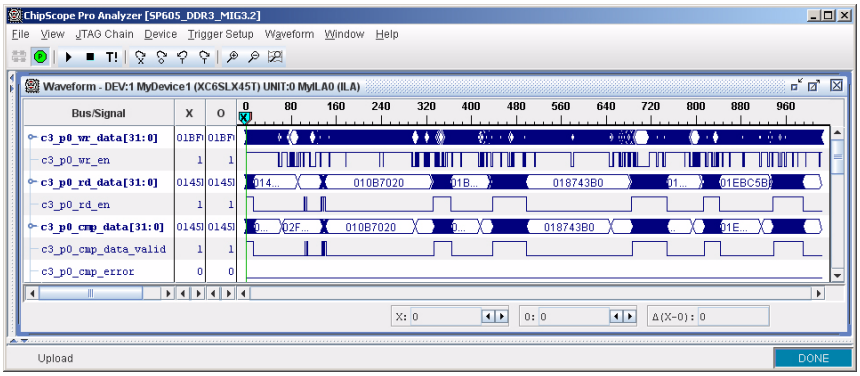

Figure 1-4: **ChipScope Pro Analyzer Tool**

For more information on the MCB, see the *Spartan-6 FPGA Memory Controller User Guide* [Ref 12]. For information about the ChipScope Pro Analyzer tool, refer to the *ChipScope Pro Software and Cores User Guide* [Ref 14].

Integrated Block for PCI Express Design

The LogiCORE™ IP Spartan-6 FPGA Integrated Endpoint Block for PCI Express® (PCIe®) core is a reliable, high-bandwidth, scalable serial interconnect building block for use with Spartan-6 FPGA devices. The Integrated Endpoint Block solution supports a 1-lane configuration that is protocol-compliant and electrically compatible with the *PCI Express Base Specification v1.1*.

The Integrated Endpoint Block solution is compatible with industry-standard application form factors such as the *PCI Express Card Electromechanical (CEM) v1.1* and the *PCI Industrial Computer Manufacturers Group (PICMG) 3.4* specifications.

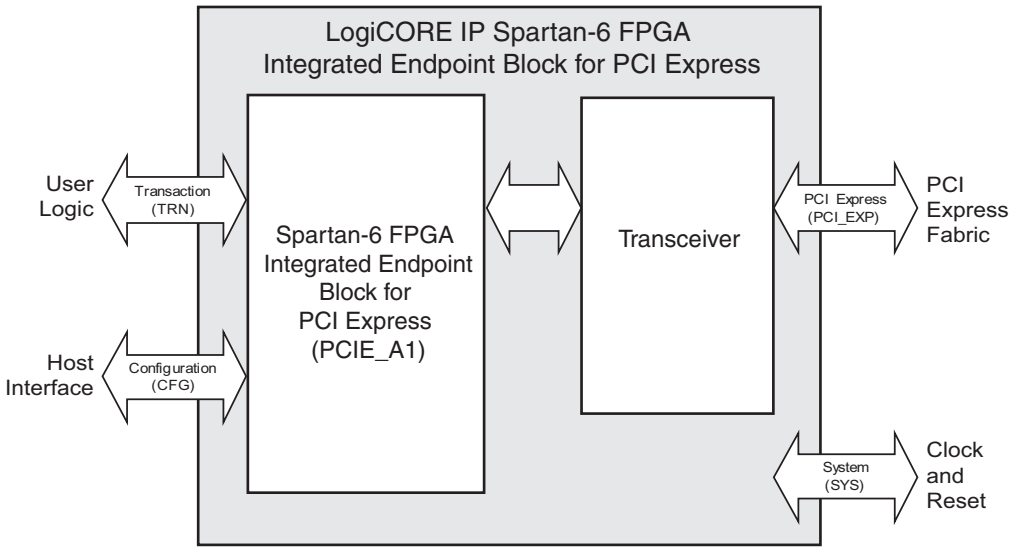

Figure 1-5: **Integrated Endpoint Block for PCIe Top-level Functional Blocks and Interfaces**

Xilinx provides a Spartan-6 FPGA Endpoint solution for PCI Express to configure the Integrated Endpoint Block and includes additional logic to create a complete Endpoint solution for PCIe. This Xilinx Endpoint Block Wrapper for PCIe simplifies the design process and reduces time-to-market. Many easy-to-use features and optimal configuration for Endpoint applications are available at no additional cost. See the Spartan-6 FPGA Integrated Endpoint Block for PCI Express product page for more information.

The SP605 provides a 1-lane PCIe edge connector for Endpoint applications. A tutorial and design file describes how to use the CORE Generator™ tool to create a PCIe Gen1 x1 LogiCORE IP block. The generated PCIe design contains a Programmed Input/Output (PIO) example that utilizes FPGA Block RAM to create a memory space accessible from the PCIe interface. A PCIe utility program, running on a PC host, is then used to query configuration space and to read and write FPGA memory over the PCIe interface.

See the *SP605 PCIe x1 Gen1 Design Creation* tutorial for more information. [Ref 20]

MultiBoot Design

Figure 1-6, page 13 illustrates the MultiBoot operation. MultiBoot is the process by which the FPGA selectively reprograms and reloads its bitstream from an attached external memory. This feature allows field updating of a stored bitstream with a new bitstream while guarding against system upsets due to an update failure. A general update process is accomplished in a five step procedure:

1. New MultiBoot image is created
2. System setup to receive the new image
3. User application erases section of Flash
4. The new image is delivered into the system's Flash
5. User application resets system

For additional information on the Spartan-6 MultiBoot feature, see the *Spartan-6 FPGA Configuration User Guide* [Ref 5]. For a demonstration of this operation on the Spartan-6 FPGA, see the *SP605 MultiBoot Reference Design* [Ref 21].

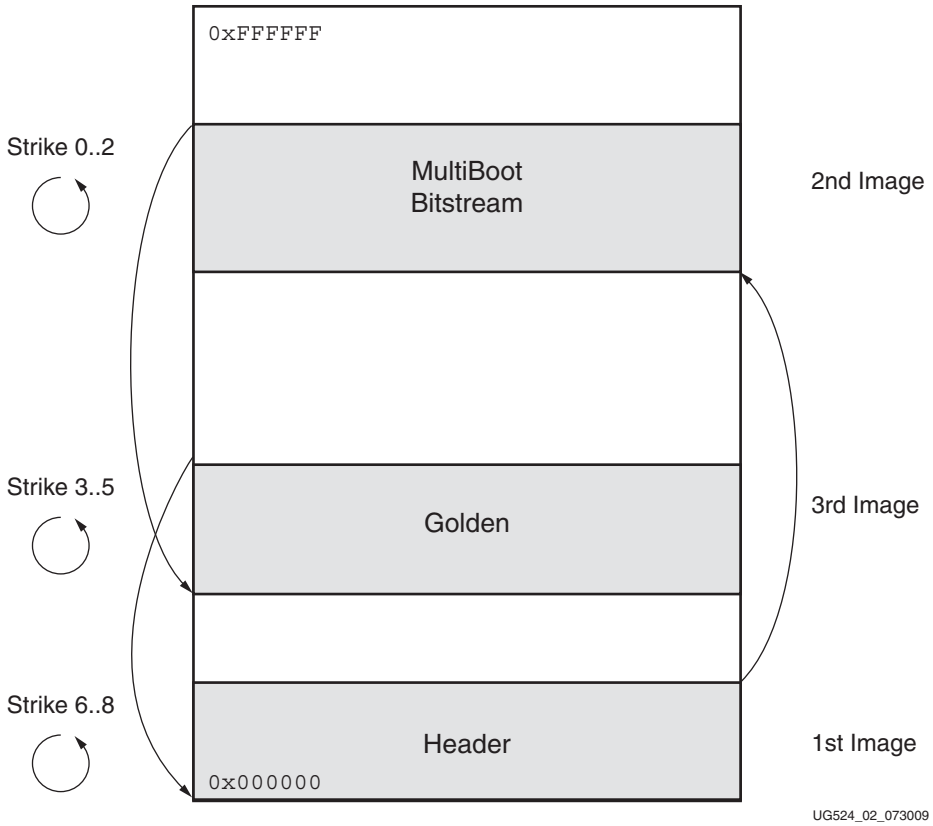

Figure 1-6: **MultiBoot Operation**

ChipScope Pro IBERT Design

The CORE Generator tool provides designers using the Spartan-6 GTP transceivers the ability to generate a hardware design containing an Integrated Bit Error Ratio Test (IBERT) core. The IBERT core instantiates a design with Spartan-6 GTP transceivers, data pattern generators, and data pattern checkers. The generated hardware design is based on user input for the device part and package, the location of a system clock pin, the desired GTP reference clock, and the expected line rate. Once configured, the IBERT design running in the FPGA is controlled through the ChipScope Pro Analyzer's IBERT Console to set GTP transceiver attributes and to exercise the high-speed serial GTP transceivers.

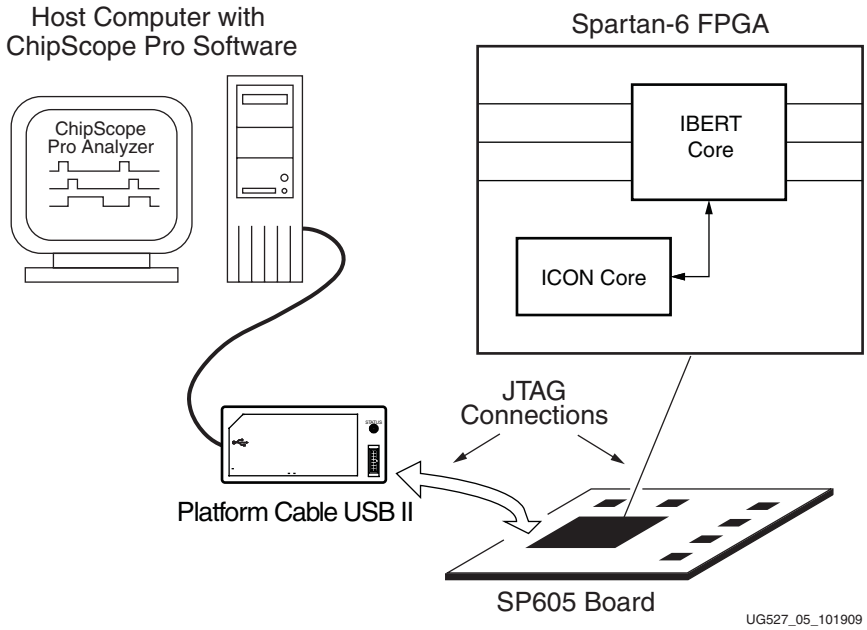

Figure 1-7: **IBERT Core Generated Using ChipScope Pro Software**

The LogiCORE IBERT designs verify loopback connections over the following interfaces that use the GTP transceivers:

- SFP
- SMA
- PCIe
- FMC-LPC

The SP605 GTP IBERT Design Creation tutorials and accompanying reference designs illustrate how to use the CORE Generator tool and the ChipScope Pro Analyzer software to exercise the SP605 GTP transceivers. [Ref 22]

For information about the ChipScope Pro Analyzer tool, refer to the *ChipScope Pro Software and Cores User Guide*. [Ref 14]

Base Reference Design

An image processing and networking application is shown through the base reference design provided with the SP605 Evaluation Kit . *Getting Started with the Xilinx Spartan-6 FPGA SP605 Evaluation Kit* describes the components of the base reference design application and how to run the reference design. [Ref 2]

Stand-Alone Applications

Each feature on the board can be tested for functionality by using the on-board BIST application [Ref 18] or by using the stand-alone applications [Ref 23] offered on the SP605 reference designs Web page. The stand-alone application contains the GPIO header and Suspend/Awake feature tests.

Table 1-1: **Stand-Alone Applications**

Feature	Feature Test Capability
Spartan-6 FPGA	BIST
DDR3 Component	BIST
SPI x4 Flash	SPI Configuration Mode
Linear BPI Flash	BIST, BPI-UP Configuration Mode
10/100/1000 Ethernet PHY	BIST, Base Reference Design (BRD)
RS232 UART (USB Bridge)	BIST
IIC	BIST
Clock, socket, SMA	200 MHz system clock, 27MHz populated socket, User SMA
VITA 57.1 FMC-LPC connector	Factory Test
LEDs (Ethernet PHY)	BIST
Suspend Header/Awake LED	Web Tutorial
LEDs (INIT/DONE)	BIST
User LED	BIST
User DIP Switch	BIST
User Pushbutton	BIST
User 6-pin (4 I/O) Header	Web Tutorial
Pushbutton (PROG)	BIST
USB JTAG	Configuration
Onboard Power	BIST
System ACE CF Socket Controller	BIST
GTP RX/TX Port	IBERT Web Tutorial
SFP Connector and Cage	IBERT Web Tutorial
Video VGA	BIST

Restoring Flash Contents

The SP605 Evaluation Kit contains several non-volatile memories (Linear BPI Flash, SPI Flash, and CompactFlash card) that can be overwritten by user created designs. The *Restoring Flash Contents* tutorial [Ref 24] provides a means to re-establish the original functionality programmed into the Linear BPI Flash, SPI Flash, and the CompactFlash card.

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Appendix A

References

This section provides references to documentation supporting Spartan-6 FPGAs, tools, and IP. For additional information, see www.xilinx.com/support/documentation/index.htm.

Documents supporting the SP605 Evaluation Board:

1. DS160, *Spartan-6 Family Overview*
2. UG525, *Getting Started with the Xilinx Spartan-6 FPGA SP605 Evaluation Kit*
3. UG526, *SP605 Hardware User Guide*
4. DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*
5. UG380, *Spartan-6 FPGA Configuration User Guide*
6. UG381, *Spartan-6 FPGA SelectIO Resources User Guide*
7. UG382, *Spartan-6 FPGA User Guide: Clocking Resources*
8. UG383, *Spartan-6 FPGA Block RAM Resources User Guide*
9. UG384, *Spartan-6 FPGA Configurable Logic Block User Guide*
10. UG385, *Spartan-6 FPGA Packaging and Pinouts*
11. UG386, *Spartan-6 FPGA GTP Transceivers User Guide*
12. UG388, *Spartan-6 FPGA Memory Controller User Guide*
13. UG389, *Spartan-6 FPGA DSP48A1 Slice User Guide*
14. UG029, *ChipScope Pro Software and Cores User Guide*
15. DS614, *Clock Generator (v3.01a) Data Sheet*
16. DS643, *Multi-Port Memory Controller (MPMC) (v5.02a) Data Sheet*
17. UG138, *LogiCORE™ IP Tri-Mode Ethernet MAC v4.2 User Guide*

The following SP605 tutorials and reference design files are located at http://www.xilinx.com/products/boards/sp605/reference_designs.htm:

18. XTP062, *SP605 Built-In Self Test Flash Application* (rdf0032.zip)
19. XTP060, *SP605 MIG Design Creation* (rdf0029.zip)
20. XTP065, *SP605 PCIe x1 Gen1 Design Creation* (rdf0035.zip)
21. XTP059, *SP605 MultiBoot Design* (rdf0028.zip)
22. XTP066, *SP605 IBERT Design Creation* (rdf0036.zip)
23. XTP064, *SP605 Stand-Alone Applications* (rdf0034.zip)
24. XTP061, *SP605 Restoring Flash Contents* (rdf0030.zip, rdf0031.zip)