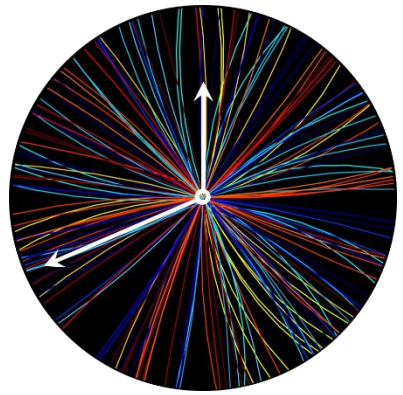


TCLink

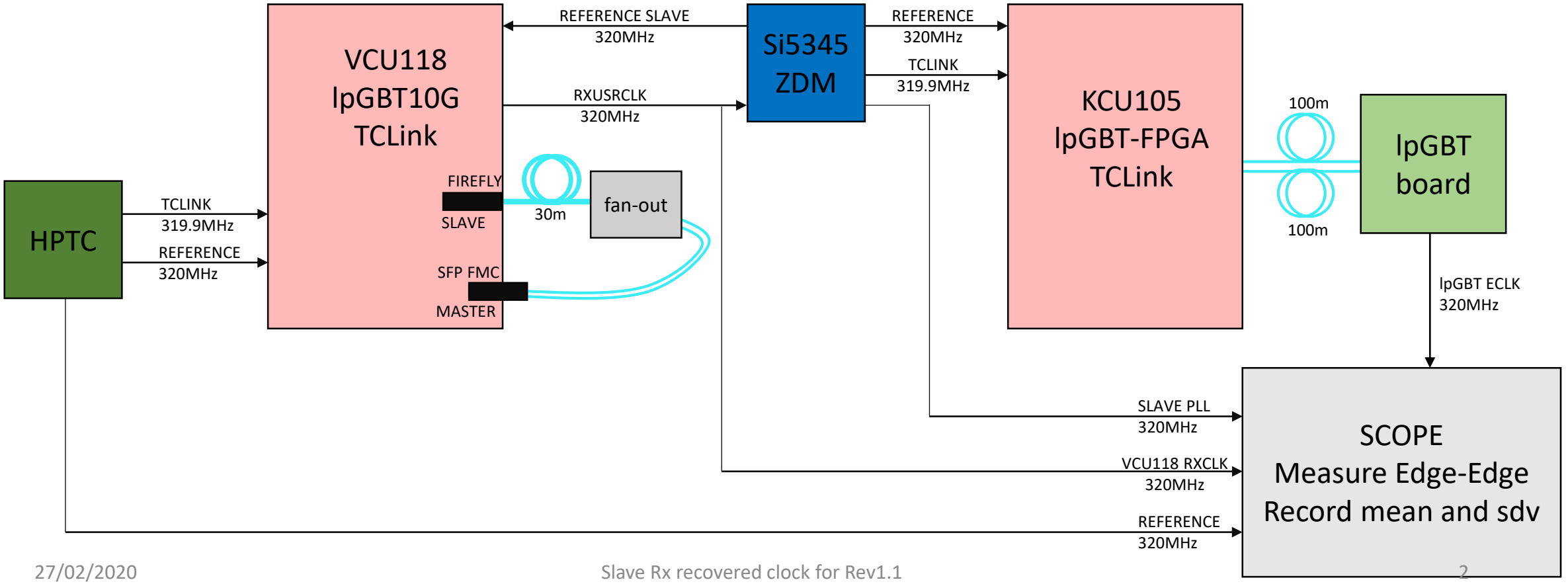
Design choice
Slave Rx recovered clock for Rev1.1

25/02/2020

Eduardo Mendes

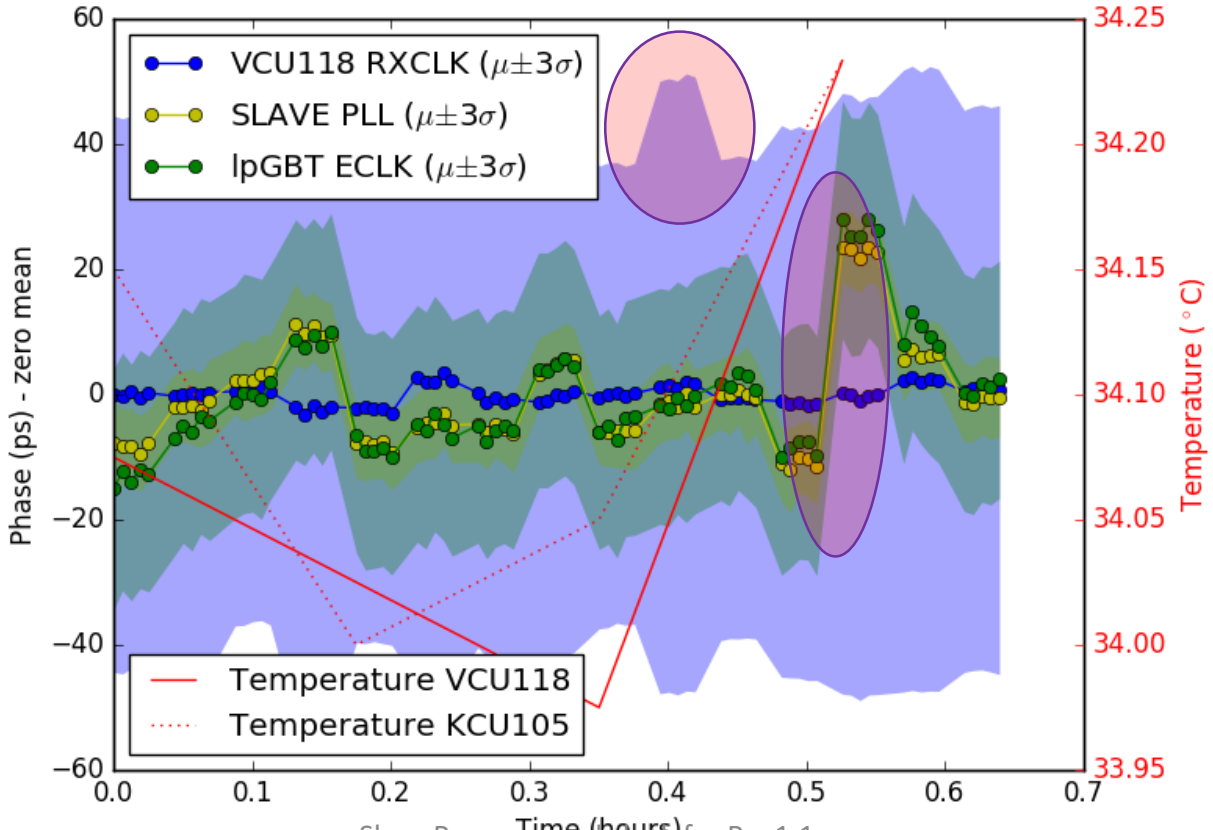
Unexpected behaviour

- During TCLink system reset tests to observe phase-determinism…



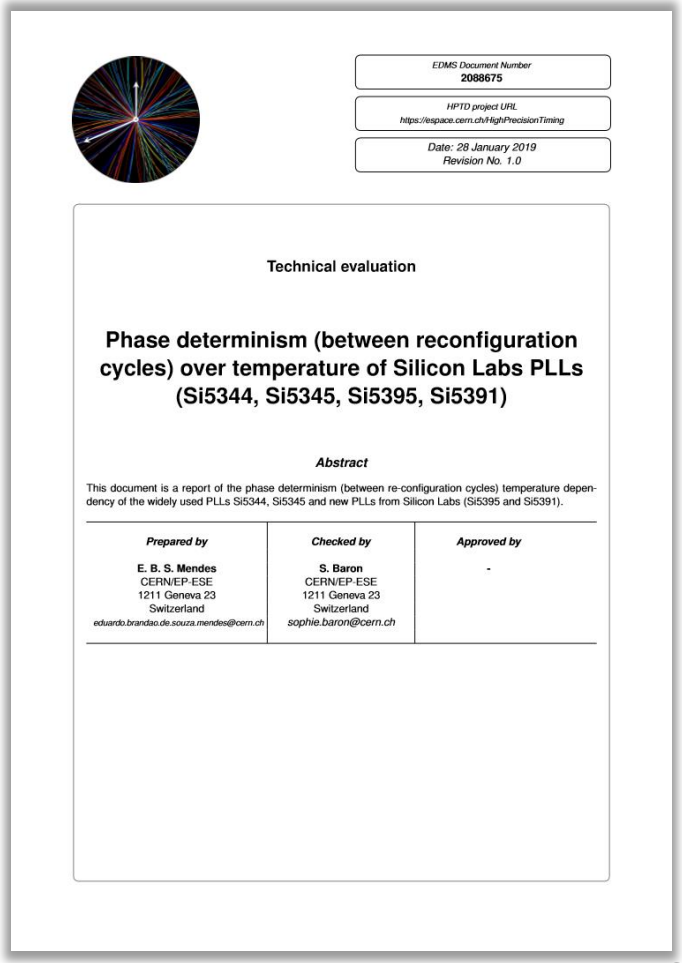
Unexpected behaviour

- …an unexpected behavior was observed with resets!
  - Phase mean jumps of clock from Si5345 and Standard deviation jumps from VCU118 clock
  - OBS: one reset of full-chain every five acquisitions



Unexpected behaviour

- This was not expected as the Si5345 PLL was heavily tested in temperature



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2088675

HPTD project URL
https://espace.cern.ch/HighPrecisionTiming

Date: 28 January 2019
Revision No. 1.0

Technical evaluation

Phase determinism (between reconfiguration cycles) over temperature of Silicon Labs PLLs (Si5344, Si5345, Si5395, Si5391)

Abstract

This document is a report of the phase determinism (between re-configuration cycles) temperature dependency of the widely used PLLs Si5344, Si5345 and new PLLs from Silicon Labs (Si5395 and Si5391).

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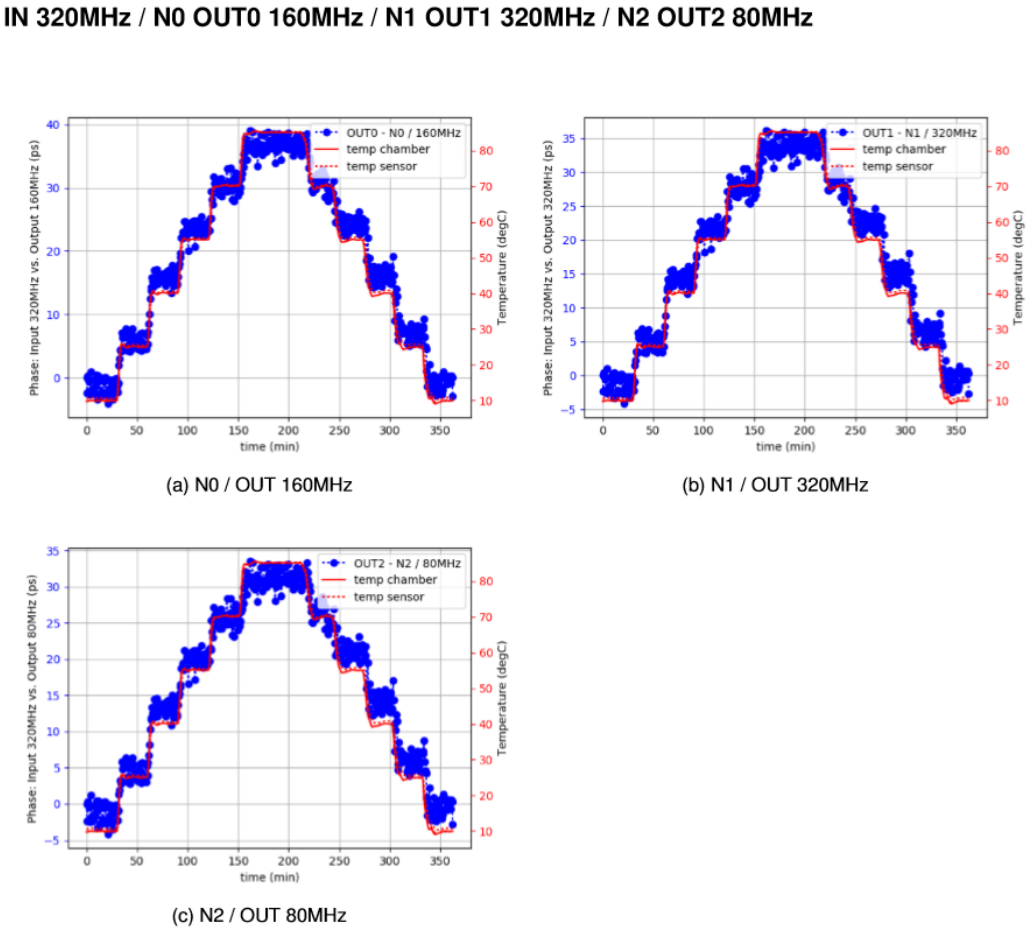
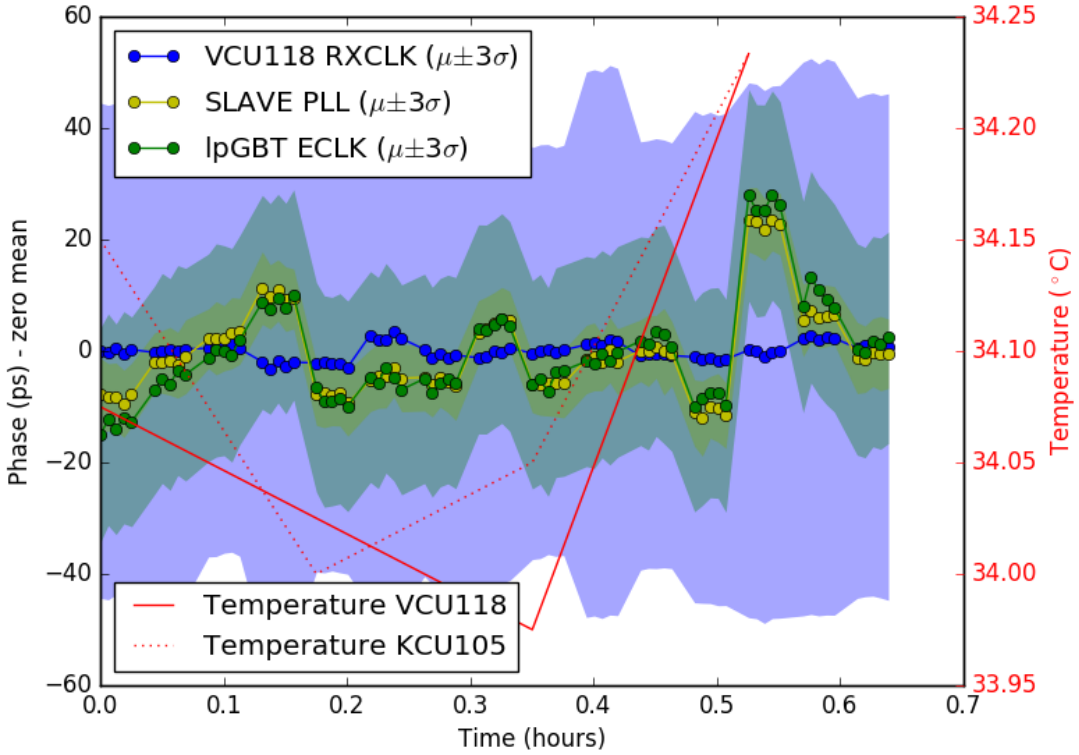
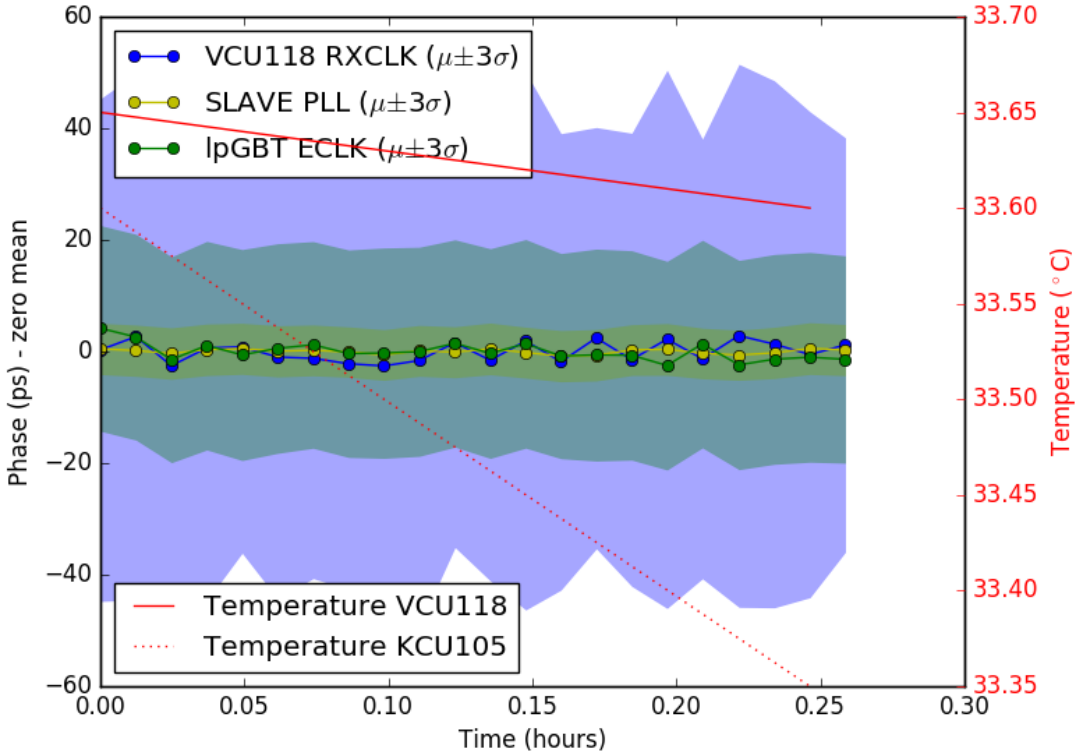


Jitter of input clock can cause a phase jump?

- Different hypothesis tried – same problem observed:
  - Shorter fibers, start resetting PLL, change zdm cable, no ddmtd clock slave/master
- Finally tested with Si5345 input as clock coming from HPTC: no problem observed



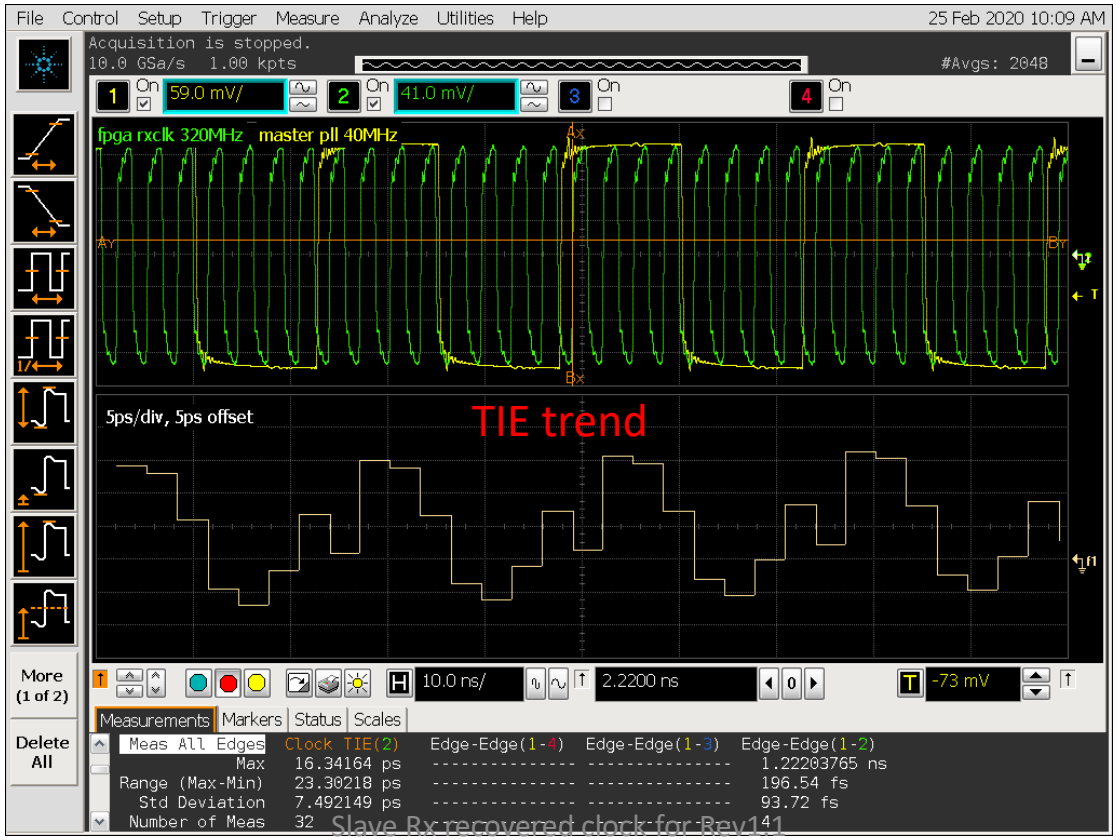
RXCLK as input of PLL



HPTC as input of PLL

TIE of RXCLK synchronized to 40MHz master PLL

- It would be unlikely a random-like jitter could cause such a phase-jump, so we decided to observe the TIE of the RXCLK synchronized to a 40MHz master PLL clock (from HPTC)
  - This is likely related to coupling between fabric (clocked at 320MHz but using a clock enable at 40MHz) and clock-tree

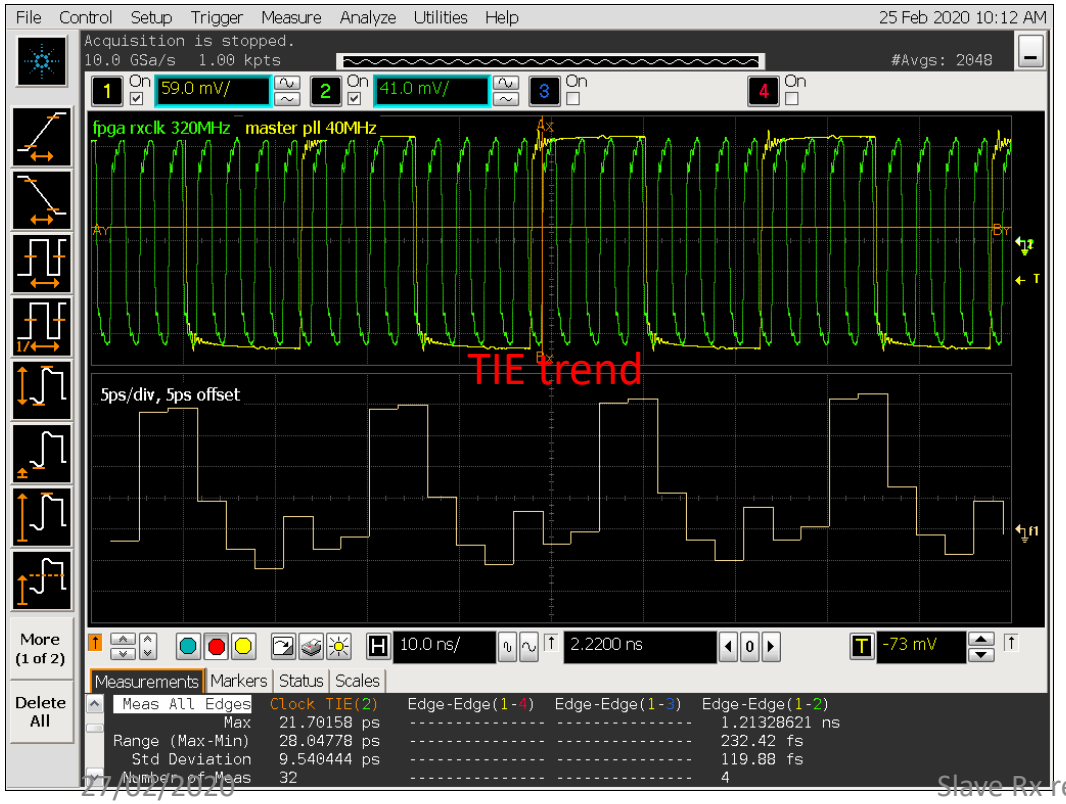


Slave Rx recovered clock for Rev141

The acquisition is averaged, so random noise is removed

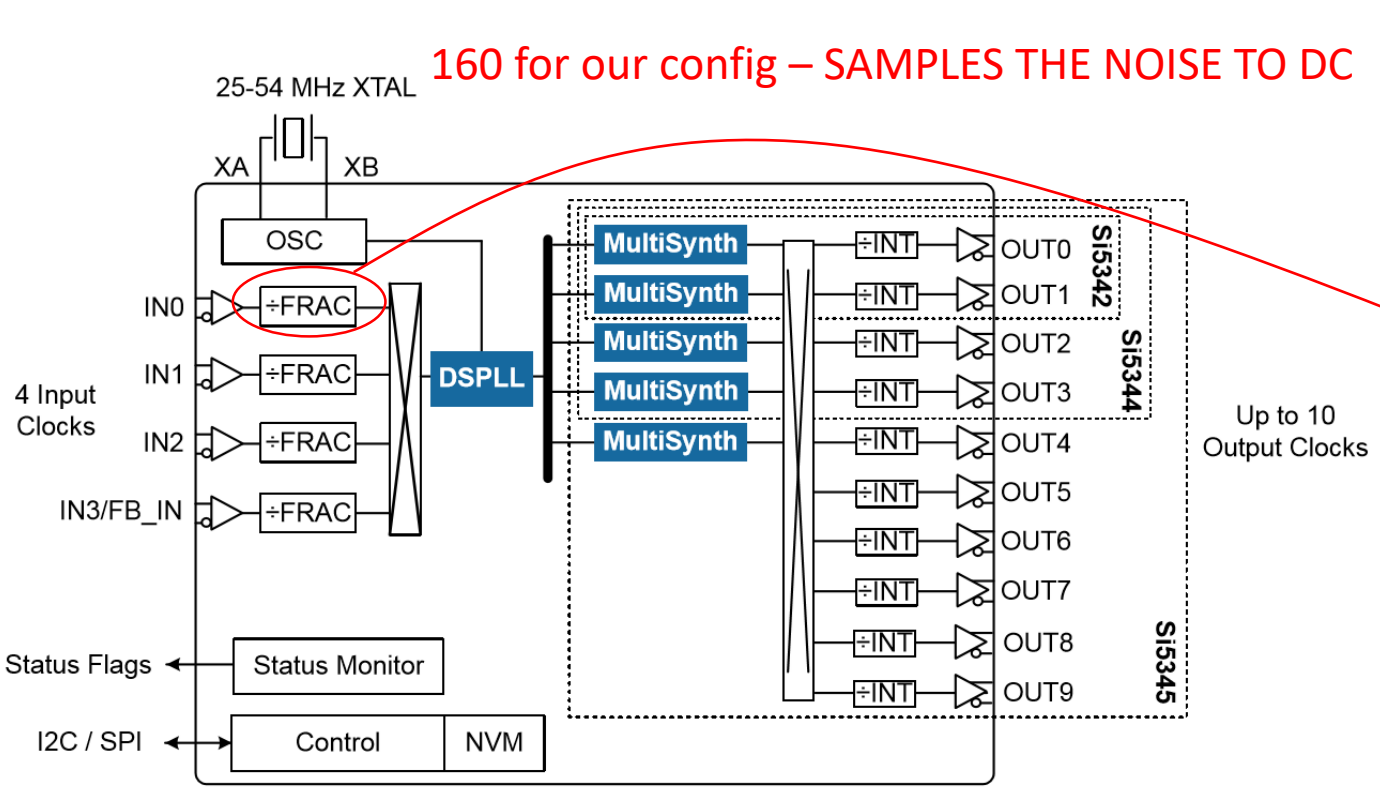
TIE of RXCLK synchronized to 40MHz master PLL

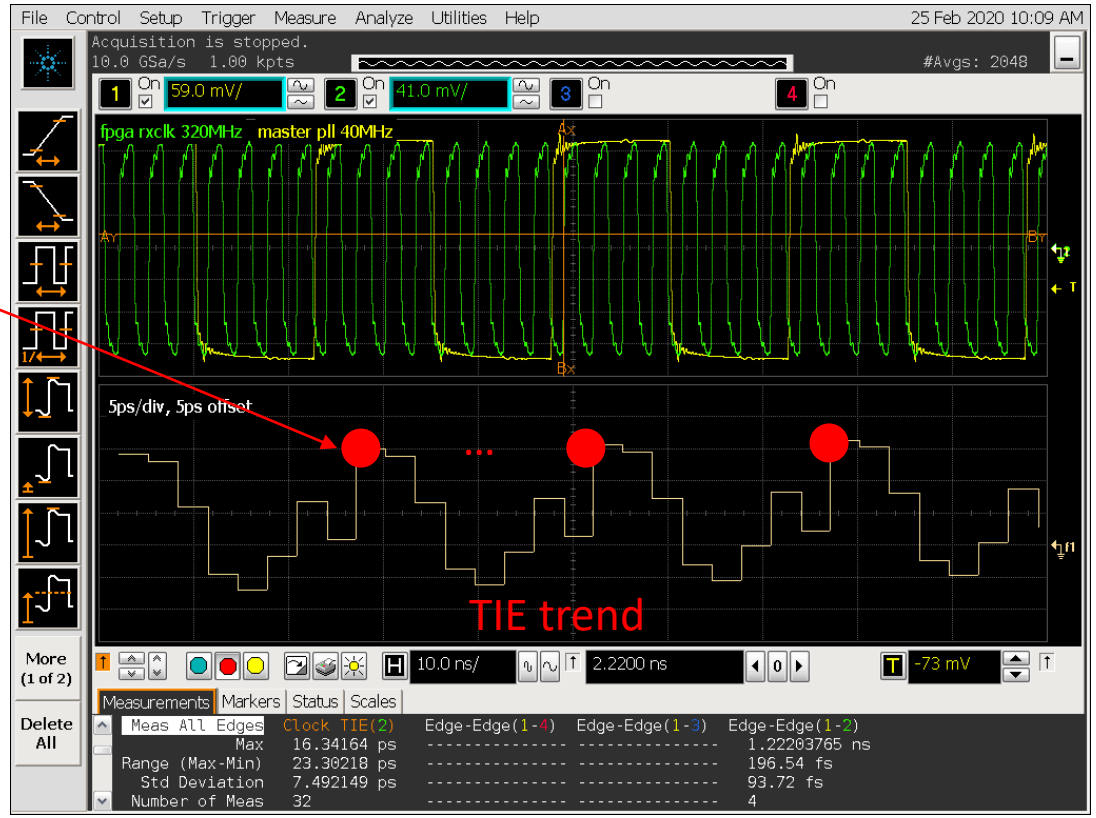
- Just by resetting the uplink logic in the fabric (i.e. not resetting the downlink at all), the TIE pattern changes:
  - Likely related to the fact that the slave Tx logic strobe is not phase-fixed with respect to the Rx logic strobe
  - This explains why the standard deviation of RXCLK changes with reset…



TIE of RXCLK synchronized to 40MHz master PLL

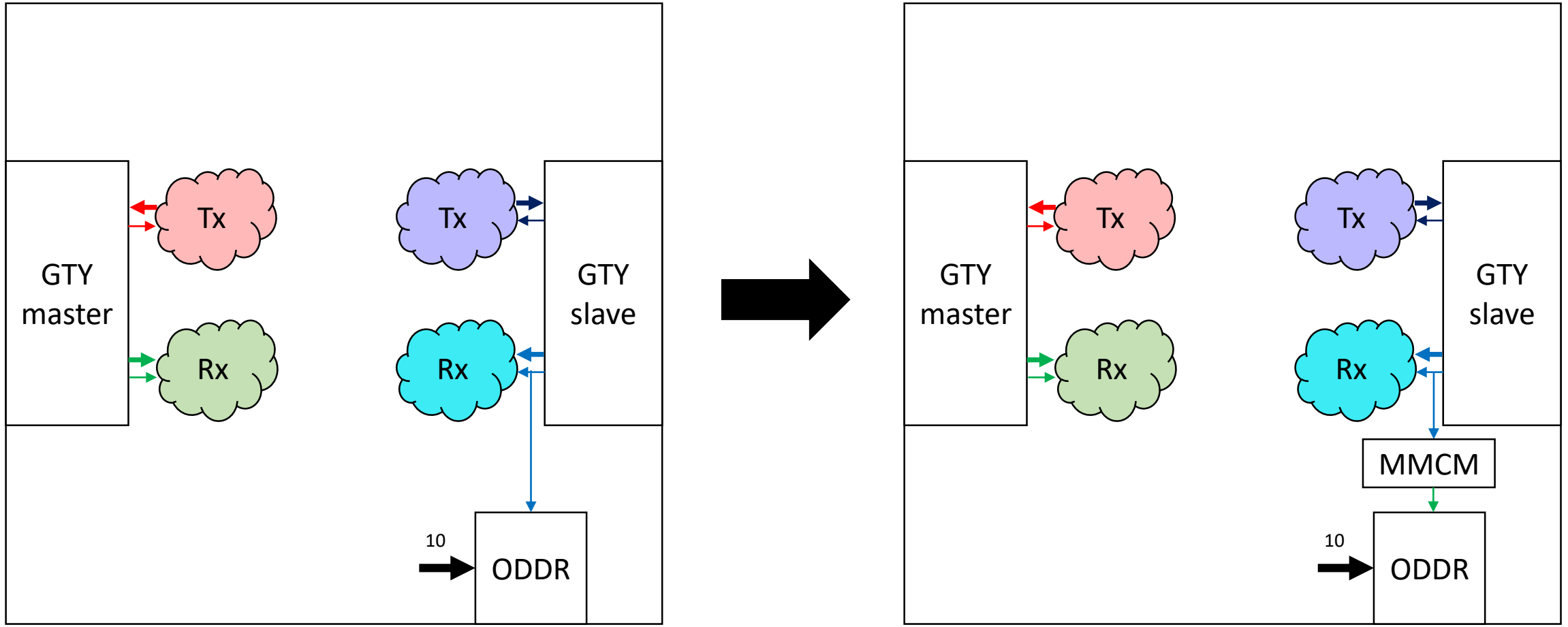
- Just by resetting the uplink logic in the fabric (i.e. not resetting the downlink at all), the TIE pattern changes:
  - … so does it explain the phase-determinism problem with the PLL





Solutions (1) – MMCM

- Dedicated MMCM could potentially filter high-frequency noise if this is being picked by the many buffers in the Rx clock-tree



Solutions (1) – MMCM

- Be careful with input divider of MMCM otherwise same problem may occur

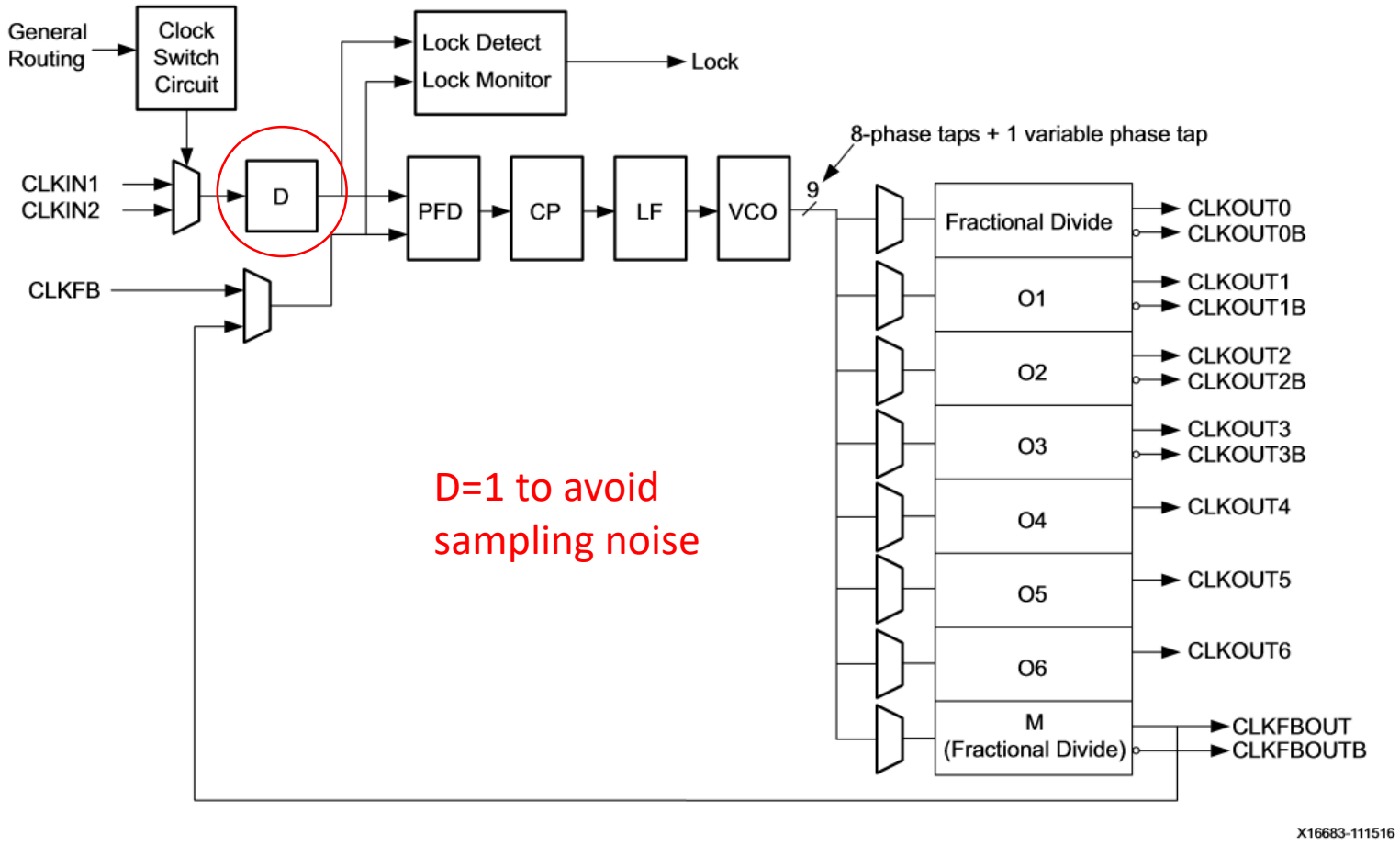
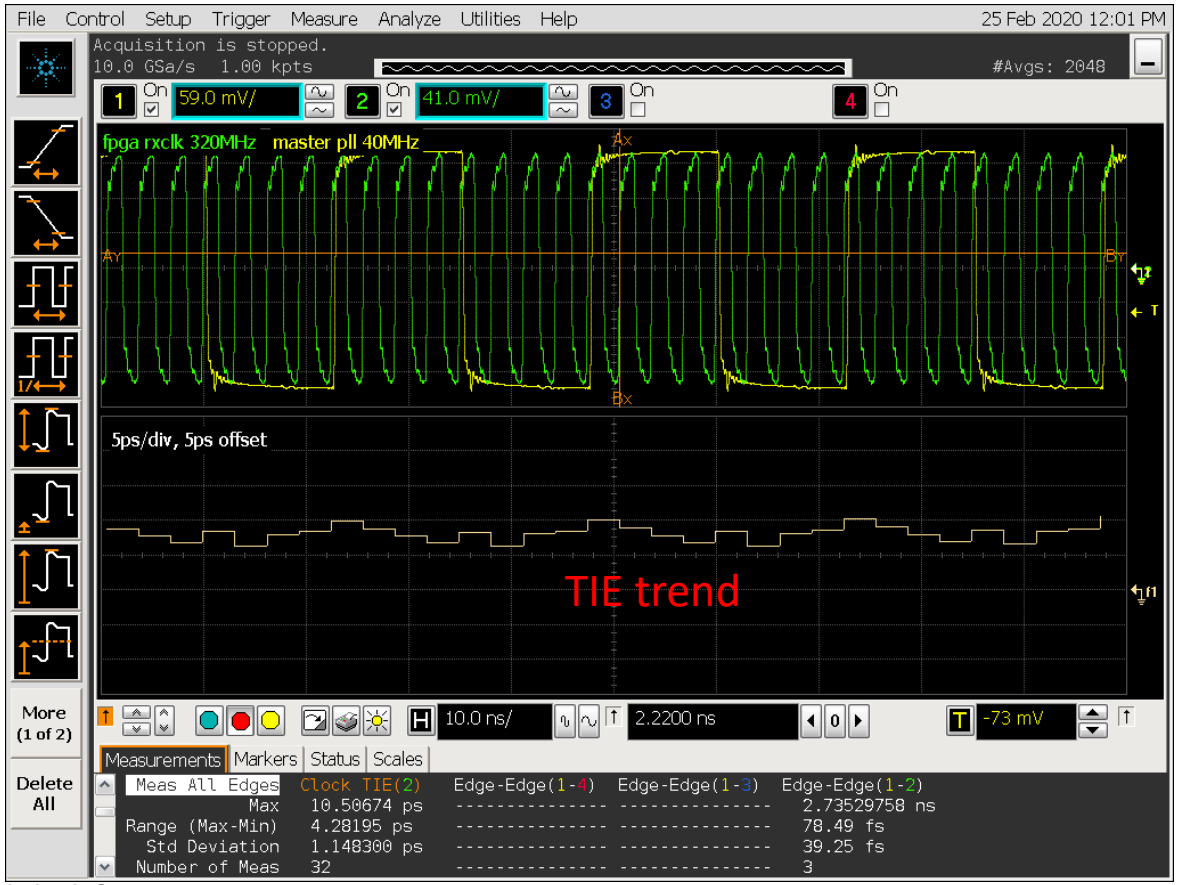


Figure 3-1: **Detailed MMCM Block Diagram**

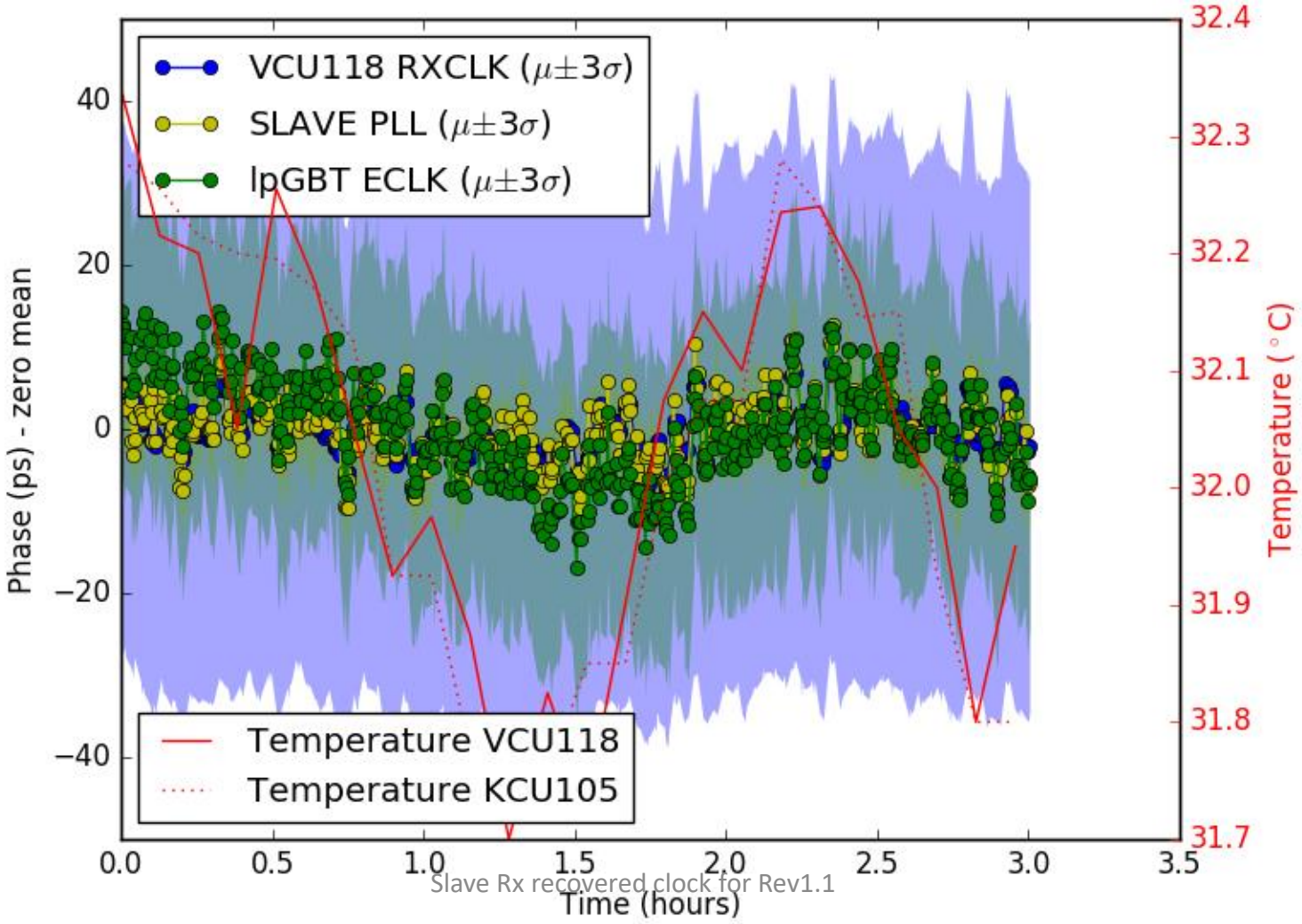
Solutions (1) – MMCM

- TIE pattern is already improved but still some remaining effect
  - Probably there is still some coupling at the ODDR/output buffer/board level



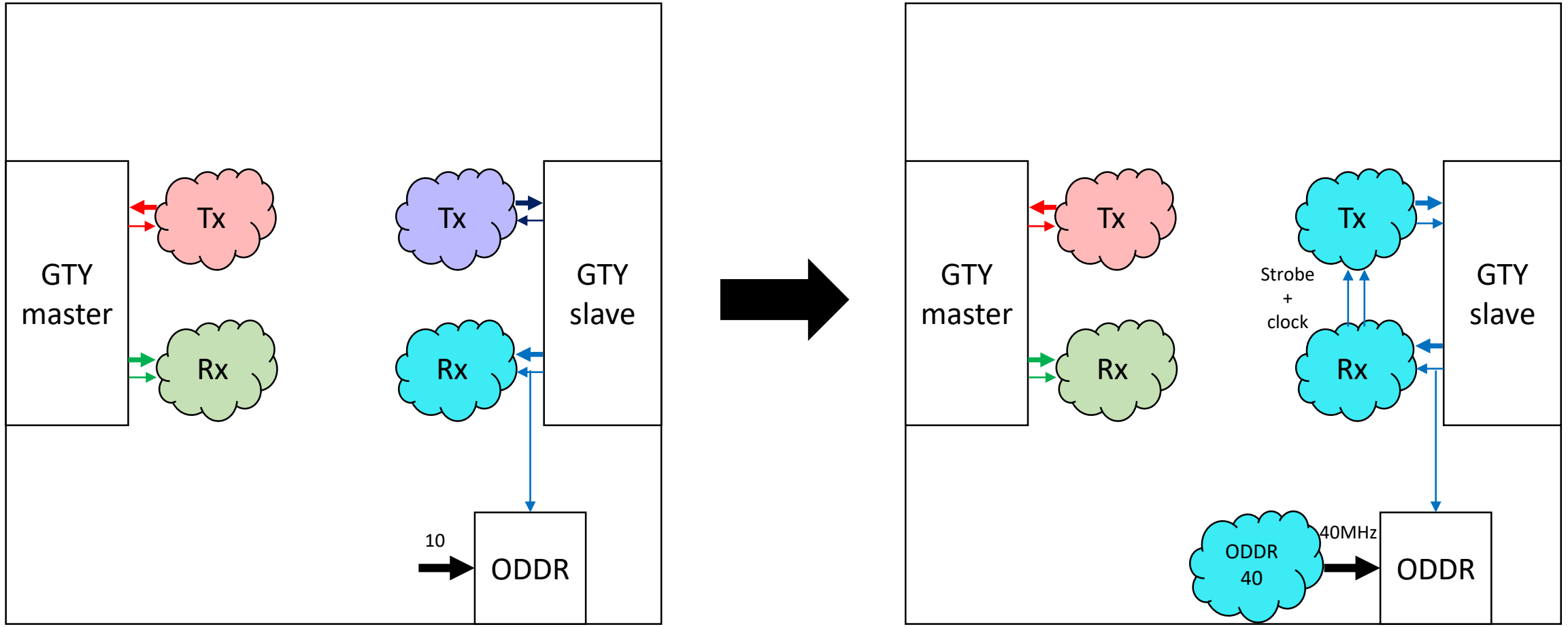
Solutions (1) – MMCM

- Quite stable results for few hours…



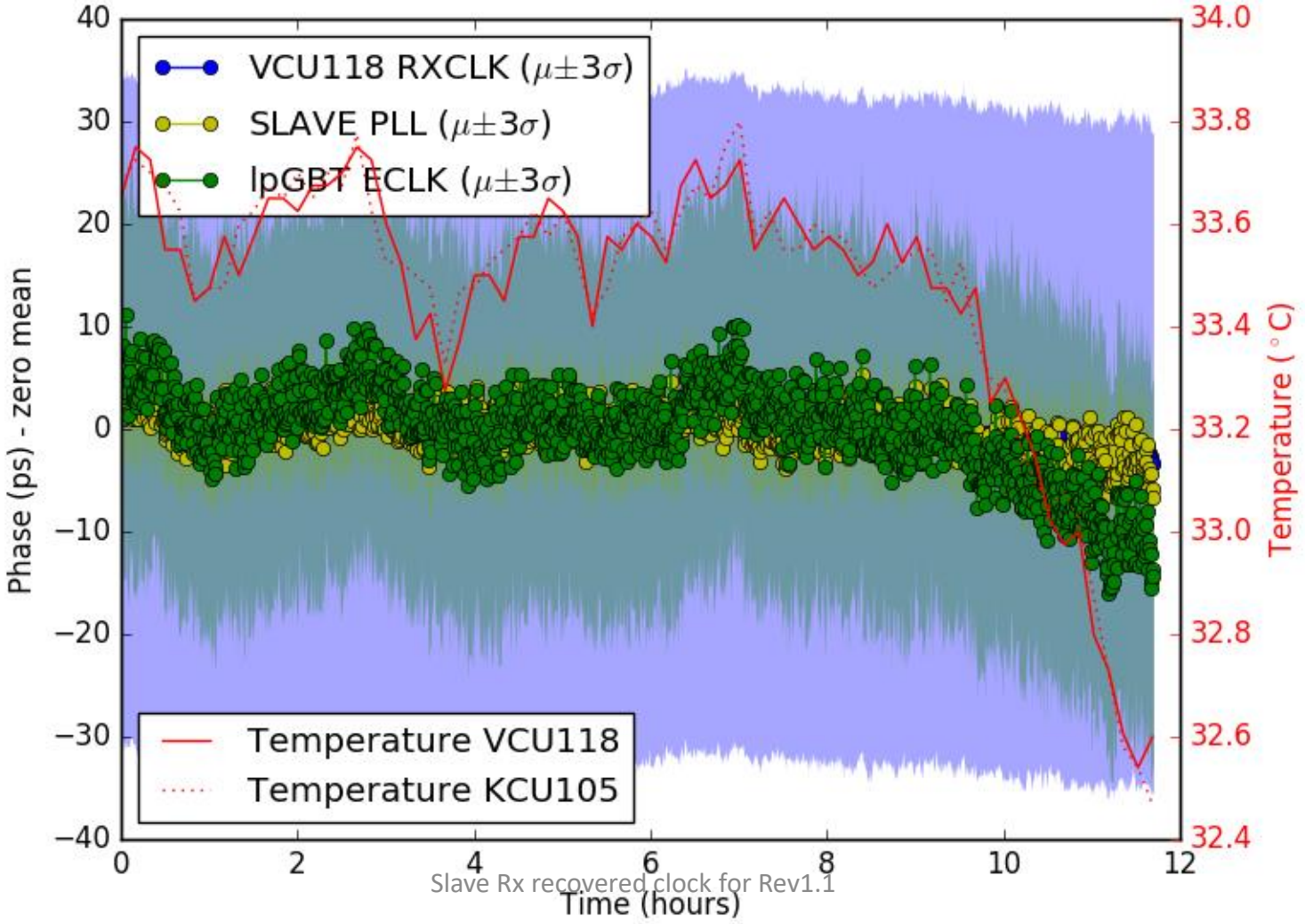
Solutions (2) – design synchronization

- Synchronize Tx/Rx strobes of slave, share rxusrclk as txusrclk and output 40MHz from ODDR



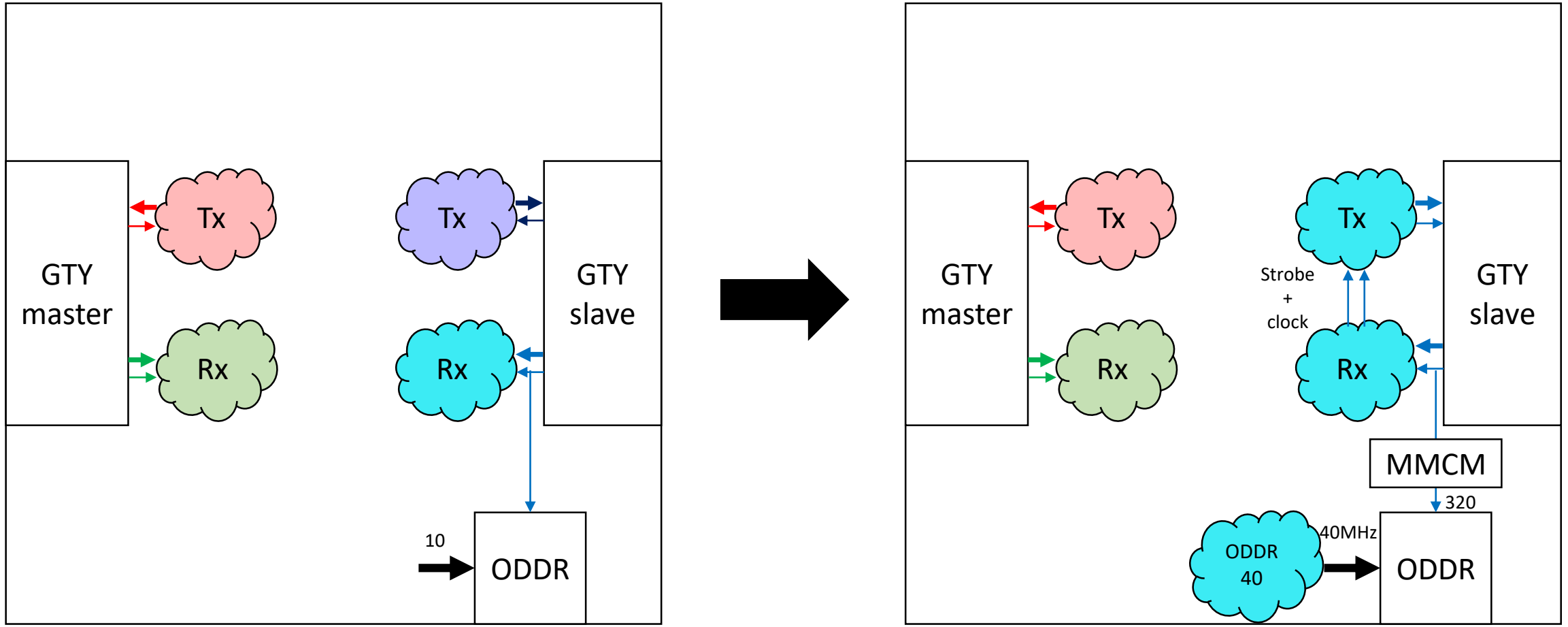
Solutions (2) – design synchronization

- Quite stable results overnight…



Preferred solution: (1+2) implemented in Rev1.1

- Improve design and makes it more resistant



Summary

- Unexpected test results from Rev1.0 during system tests
  - Coupling from fabric switching-noise to recovered clock
- Finish exhaustive tests for current system with proposed modifications
  - (1)+(2) was implemented for Rev1.1
- Then, in the future, the following tests shall be made to the design
  - Multilink design for VCU118 master (put as many MGT as possible)
  - Insert logic in the fabric to stress the design further (similar to what Jean-Pierre did)...
  - Put everything on a huge climate chamber downstairs and conclude on results...