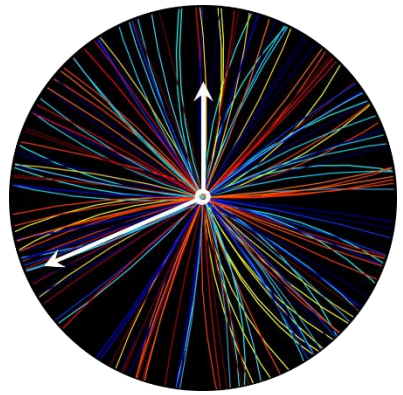


TCLink

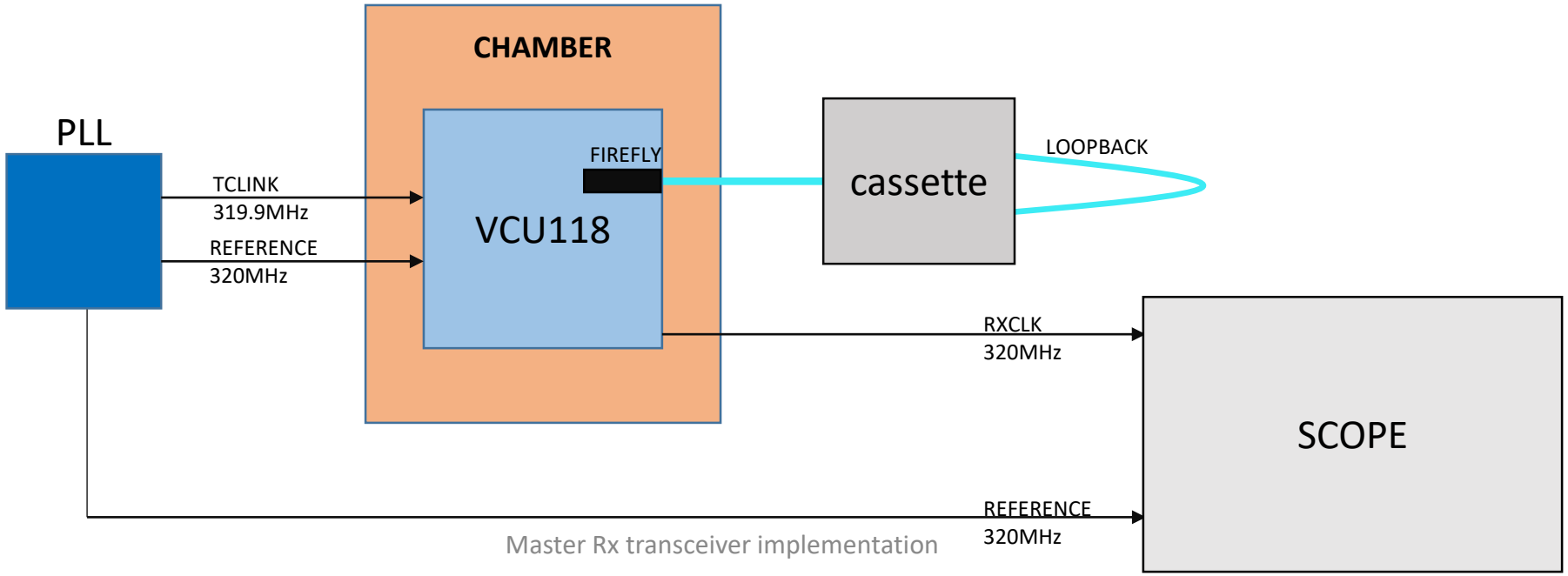
Design choice
Master Rx transceiver implementation

25/02/2020

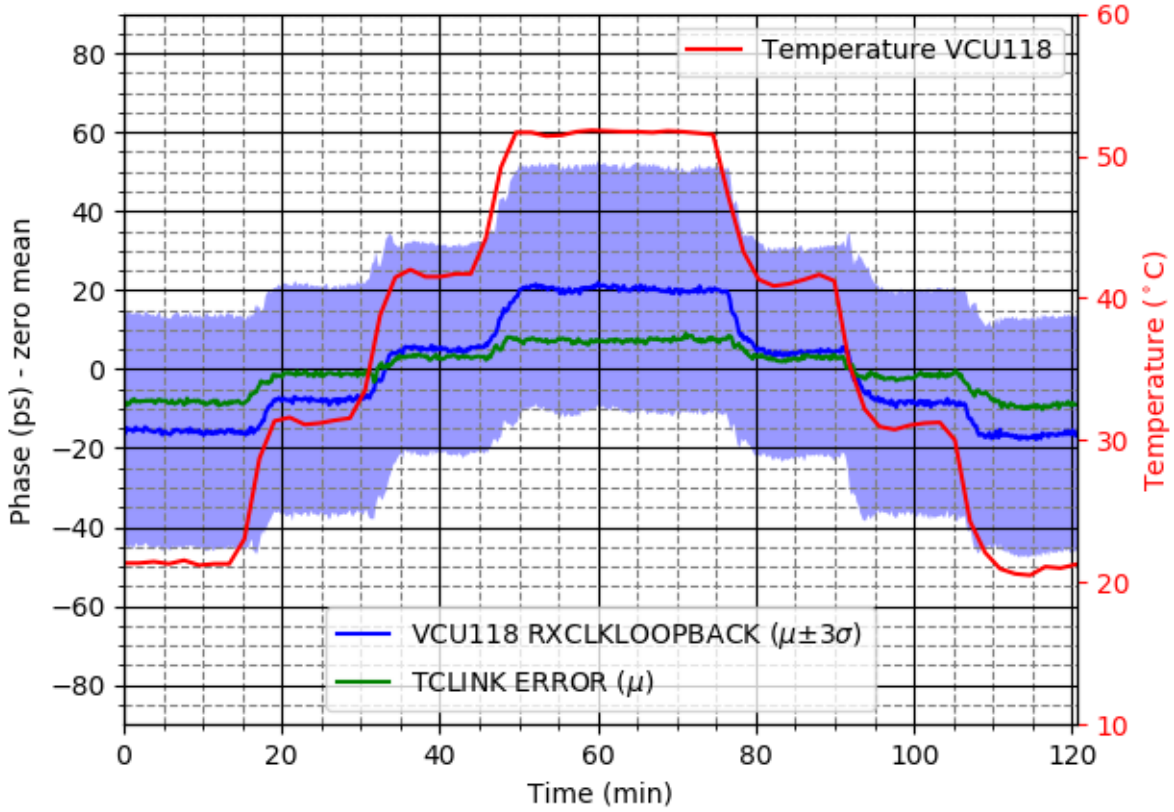
Eduardo Mendes

Objective

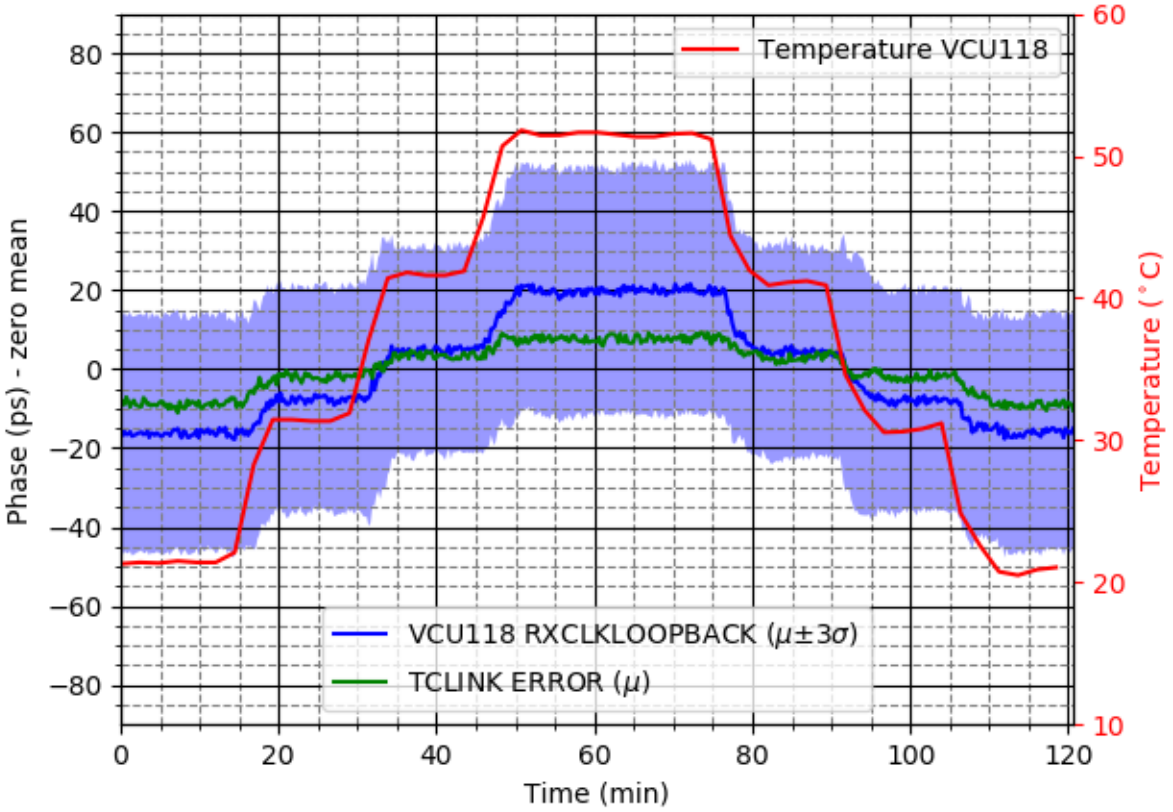
- Objective:
  - (1) Validate TCLink phase-determinism of slave
  - (2) Validate TCLink technique to deal with non fixed-latency master
  - (3) What is the best configuration for GTY master receiver?



(1) BUFFER-BYPASS – SLIDE PMA

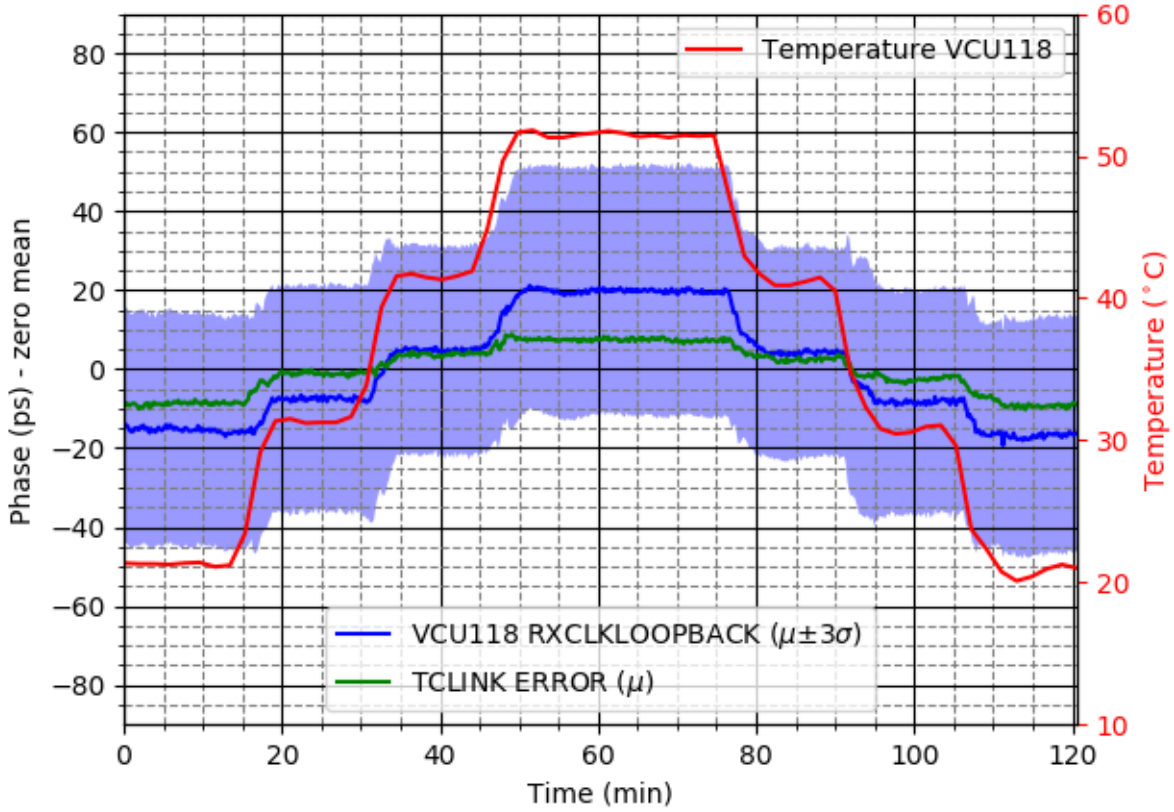


NO RESET

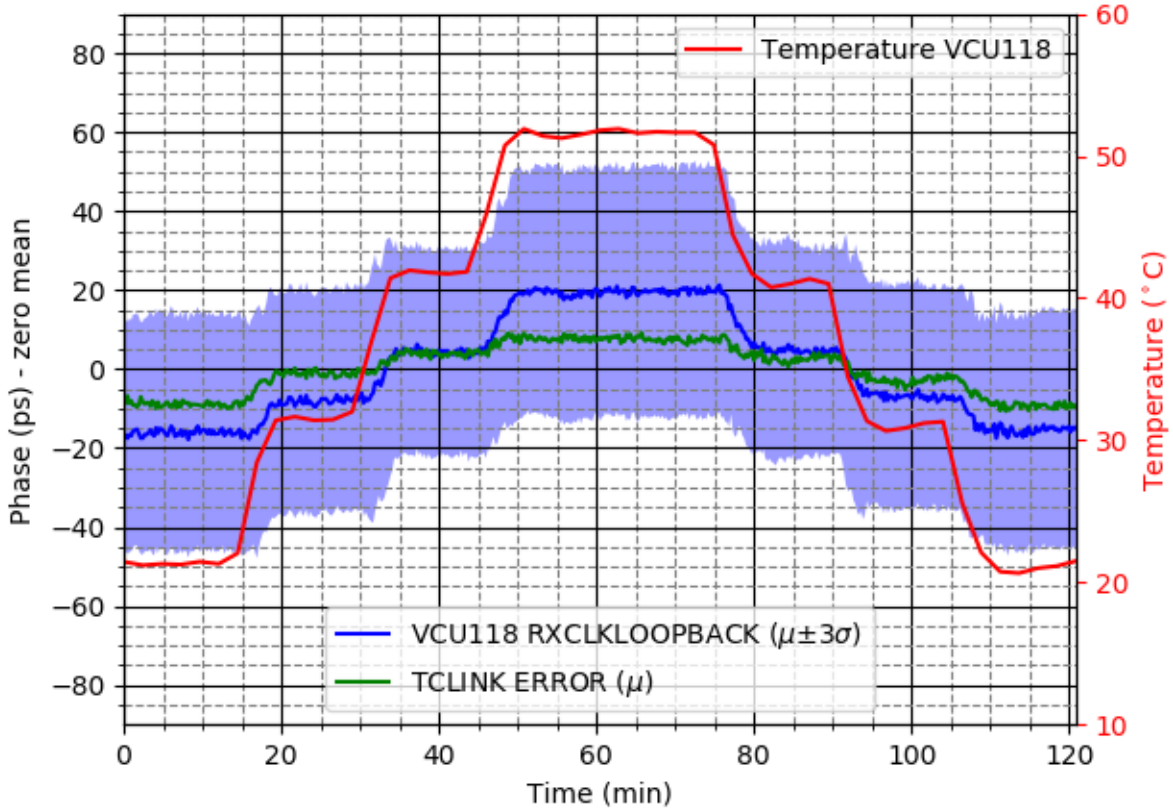


RESET

(1) BUFFER-BYPASS – ROULETTE



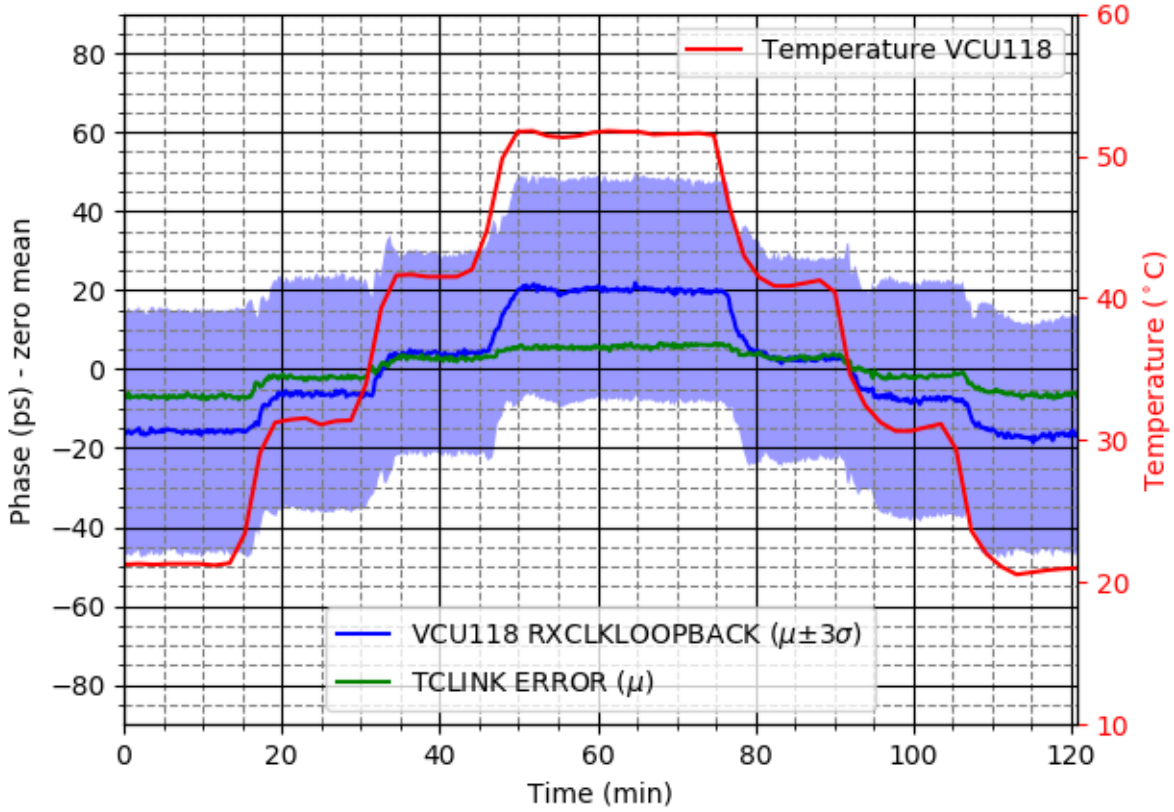
NO RESET



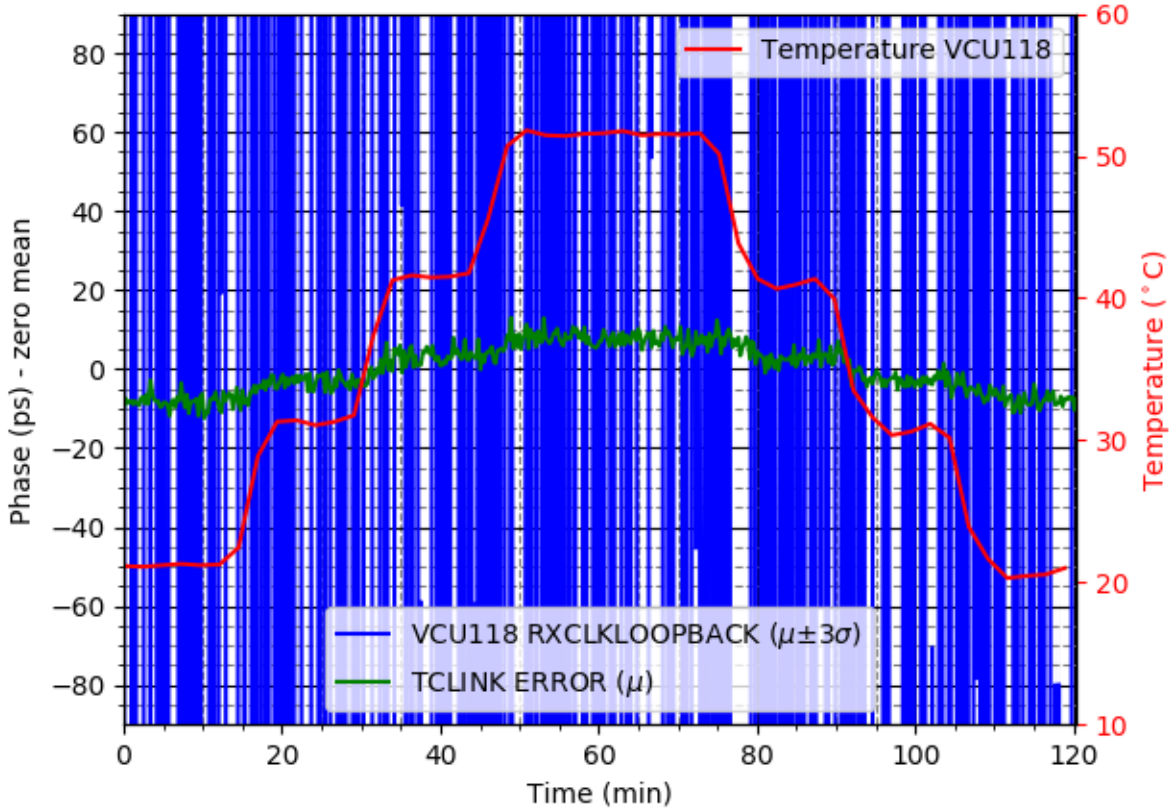
RESET

(2/3) BUFFER-BYPASS – SLIDE PCS RXOUTCLKPMA

The Rx clock itself is not fixed for the master but the error in TCLink is



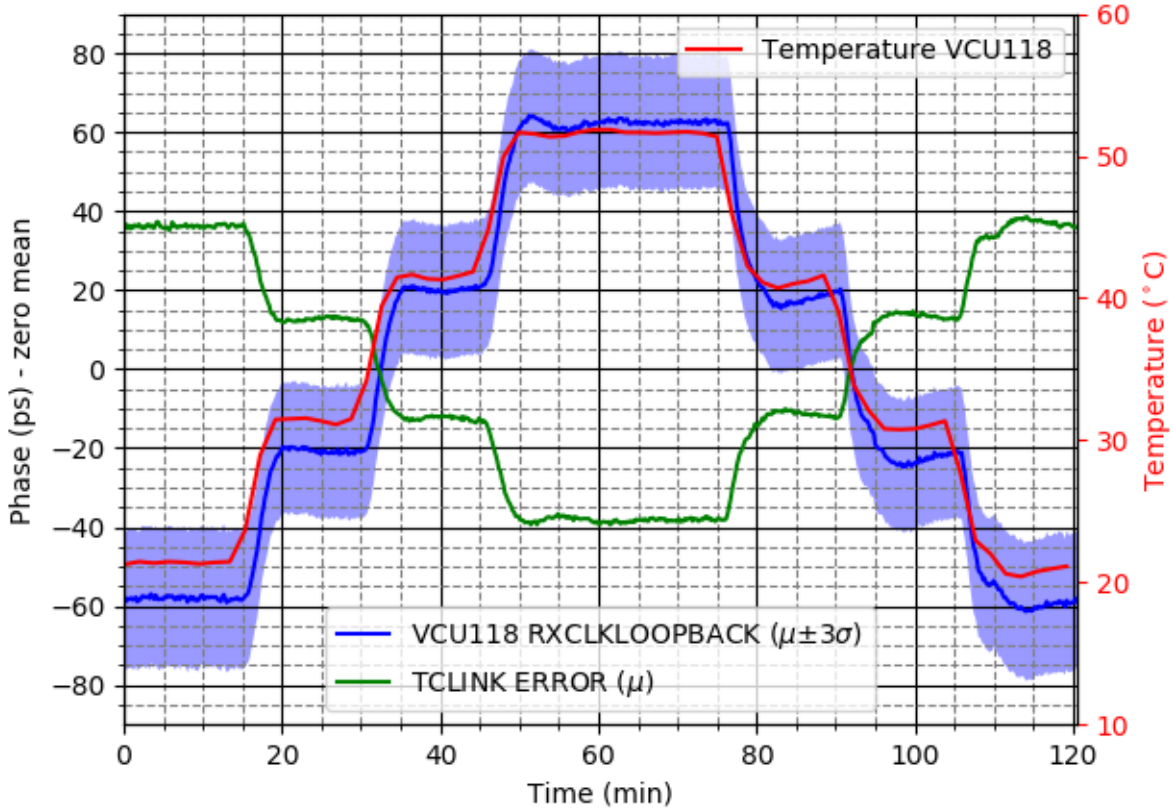
NO RESET



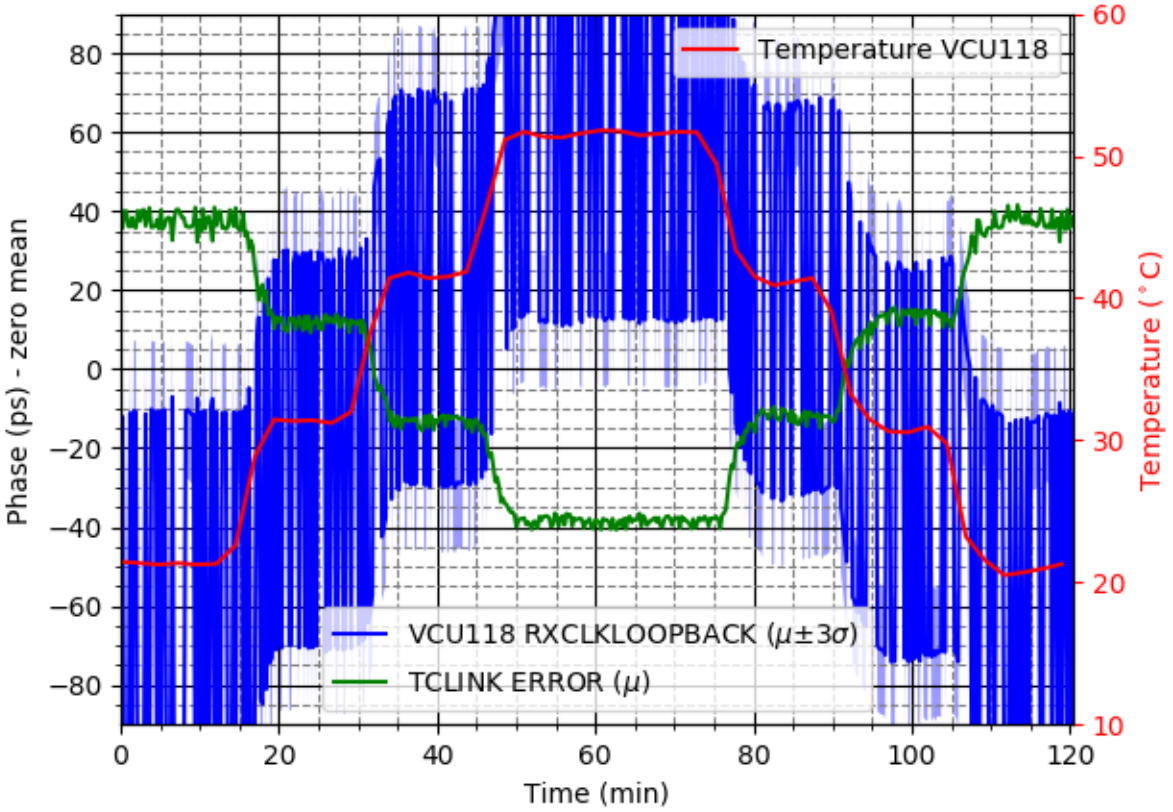
RESET

(2/3) FIFO – SLIDE PMA RXOUTCLKPCS

The Rx clock itself is not fixed for the master but the error in TCLink is



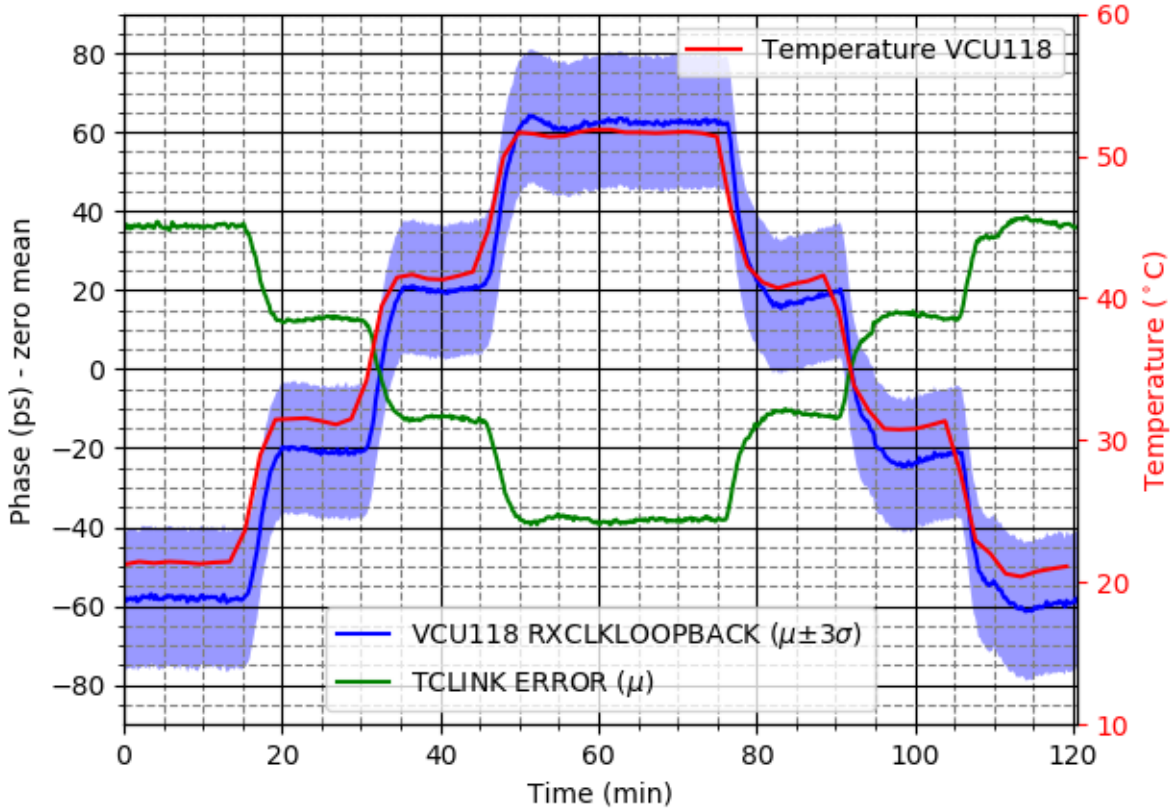
NO RESET



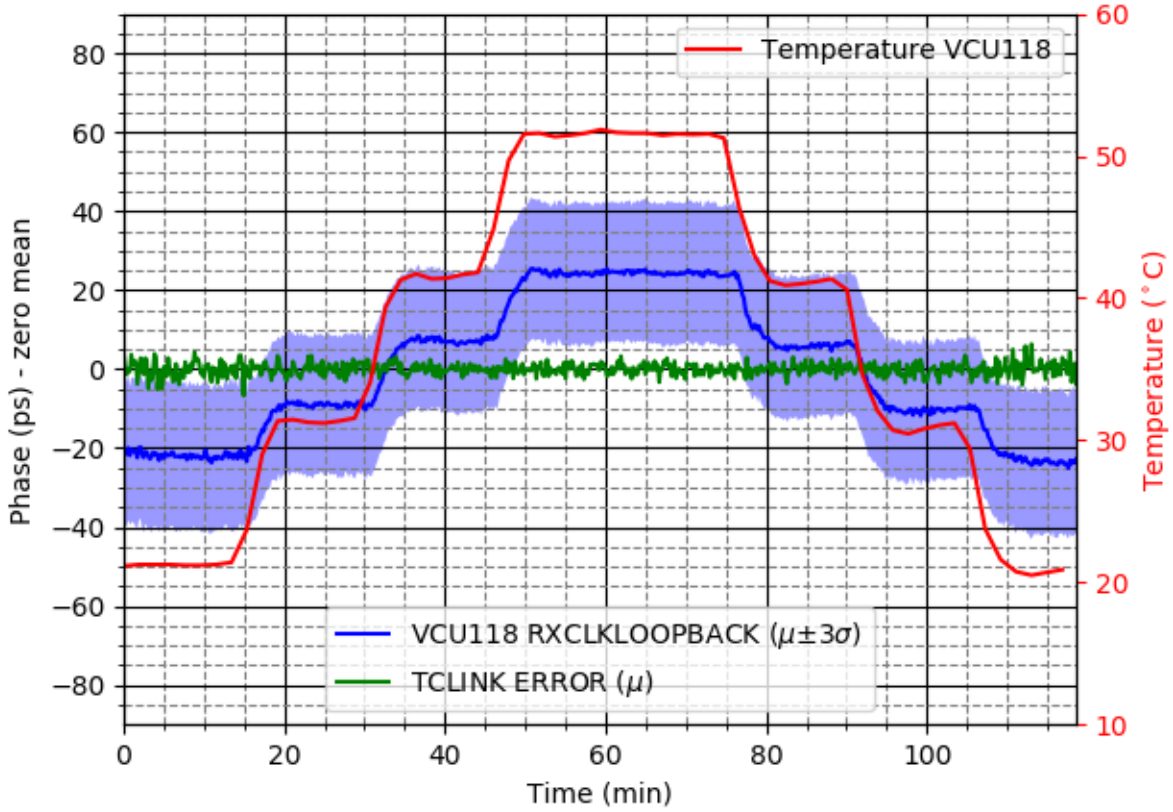
RESET

(2/3) FIFO – SLIDE PMA RXOUTCLKPCS

Illustration of TCLink compensation



NO RESET
NO COMPENSATION



NO RESET
FULL COMPENSATION

Summary

- Objective:
  - (1) Validate TCLink phase-determinism of slave
    - Fixed-latency of slave can be achieved either with buffer-bypass + slide PMA approach or roulette approach (reset until locked)
  - (2) Validate TCLink technique to deal with non fixed-latency master
    - Technique in TCLink works fine
  - (3) What is the best configuration for GTY master receiver?
    - BUFFER-BYPASS – SLIDE PCS RXOUTCLKPMA minimizes temperature variation
    - FIFO – SLIDE PCS RXOUTCLKPCS in principle is better for phase-determinism but anyway we recommend then…

BUFFER-BYPASS – SLIDE PCS RXOUTCLKPMA