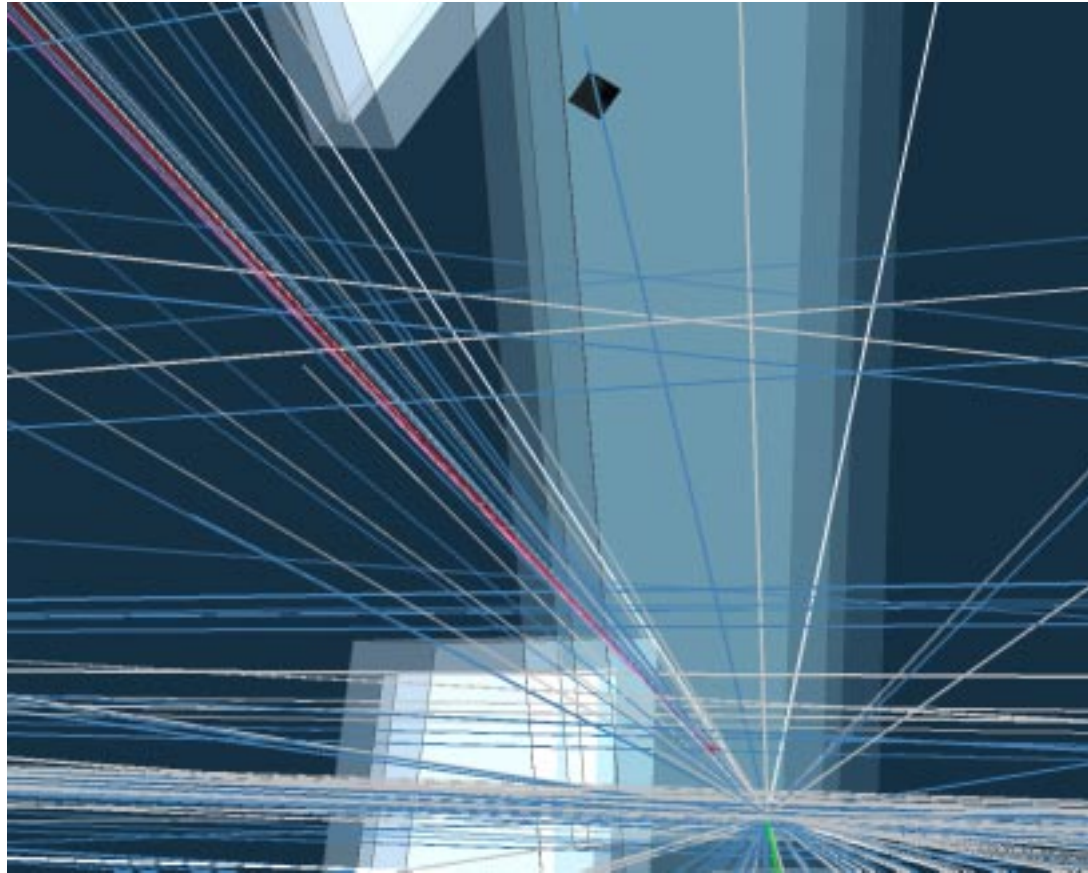


Silicon Trigger Cluster Card

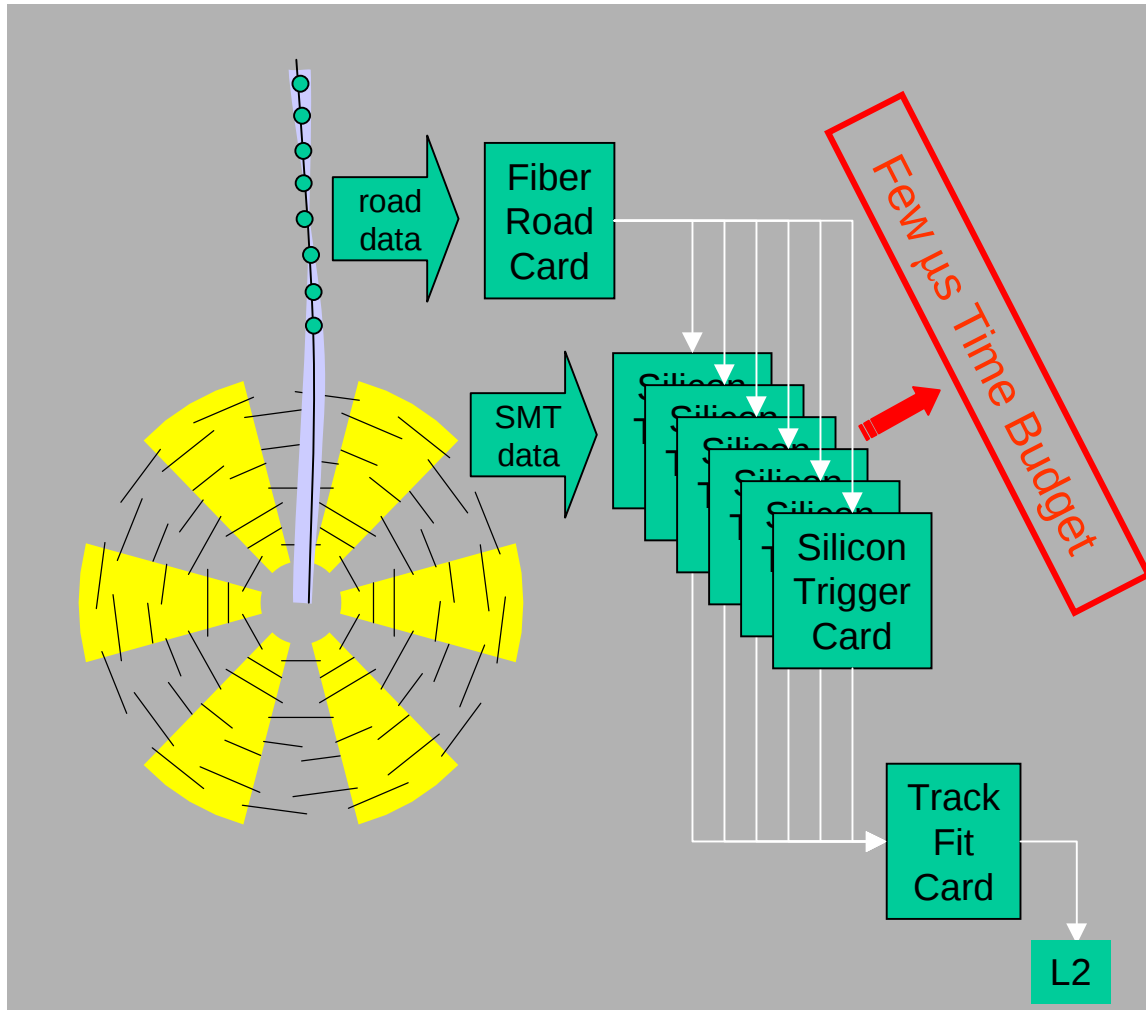


Meenakshi Narain

W. Earle, E. Hazen, U. Heintz, S. Fatakia (BU)
R. Perry, H. Wahl + engineering students (FSU)

STC Functionality

- What are we expected to do?



– Find clusters in the Silicon detector associated with the outer track

- **Inputs:**

- receive SMT data
- receive L1CTT roads

- **Functionality:**

- find hit clusters
- filter axial hits in track roads

- **Data output**

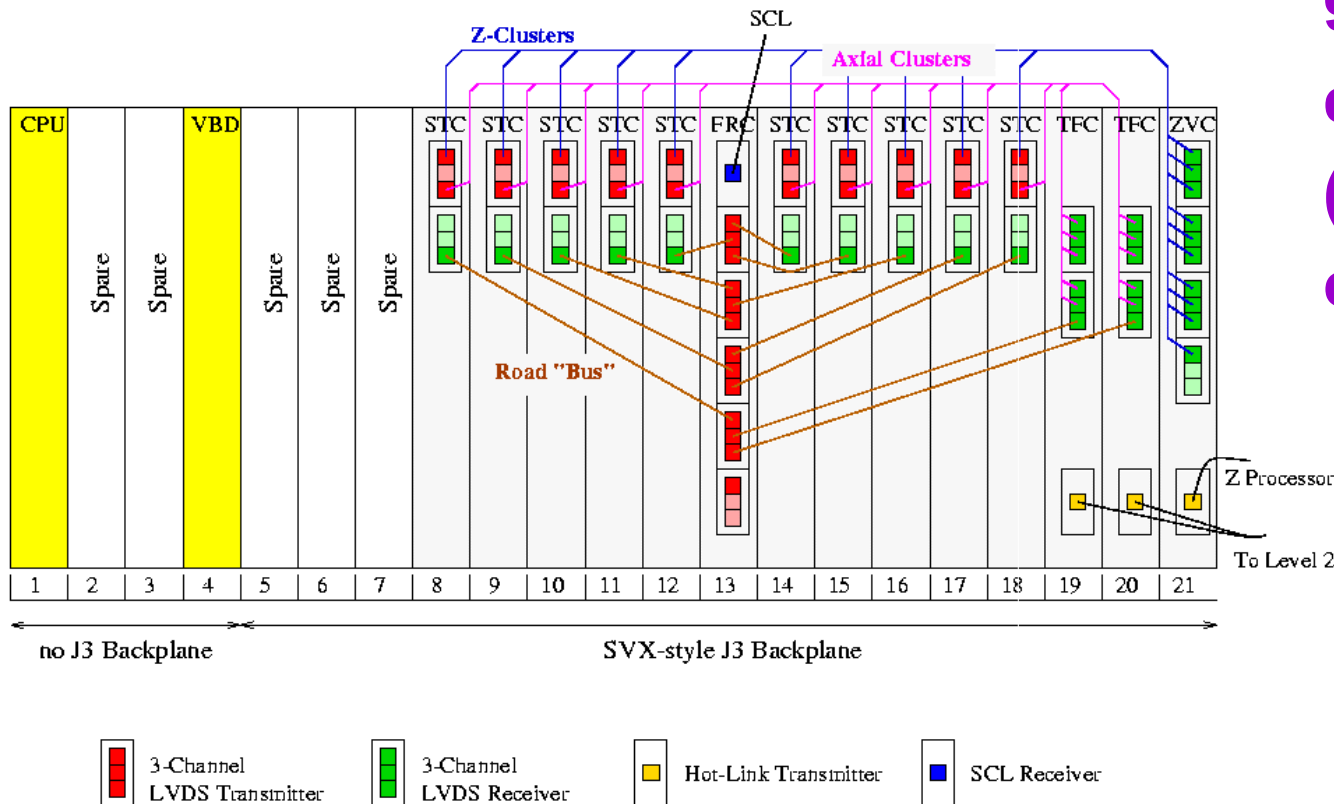
- send filtered hits to TFC
- send ALL hits to L3
- send 90° hits to ZVC
- collect stats for monitoring
- send all internal info for unbiased events

Where do we fit in?

Backplane connections not shown:
Level 3 buffering (J3 bus)
SCL Init/busy/error (J0 TBUS)
VTM Inputs (CTT, SMT)

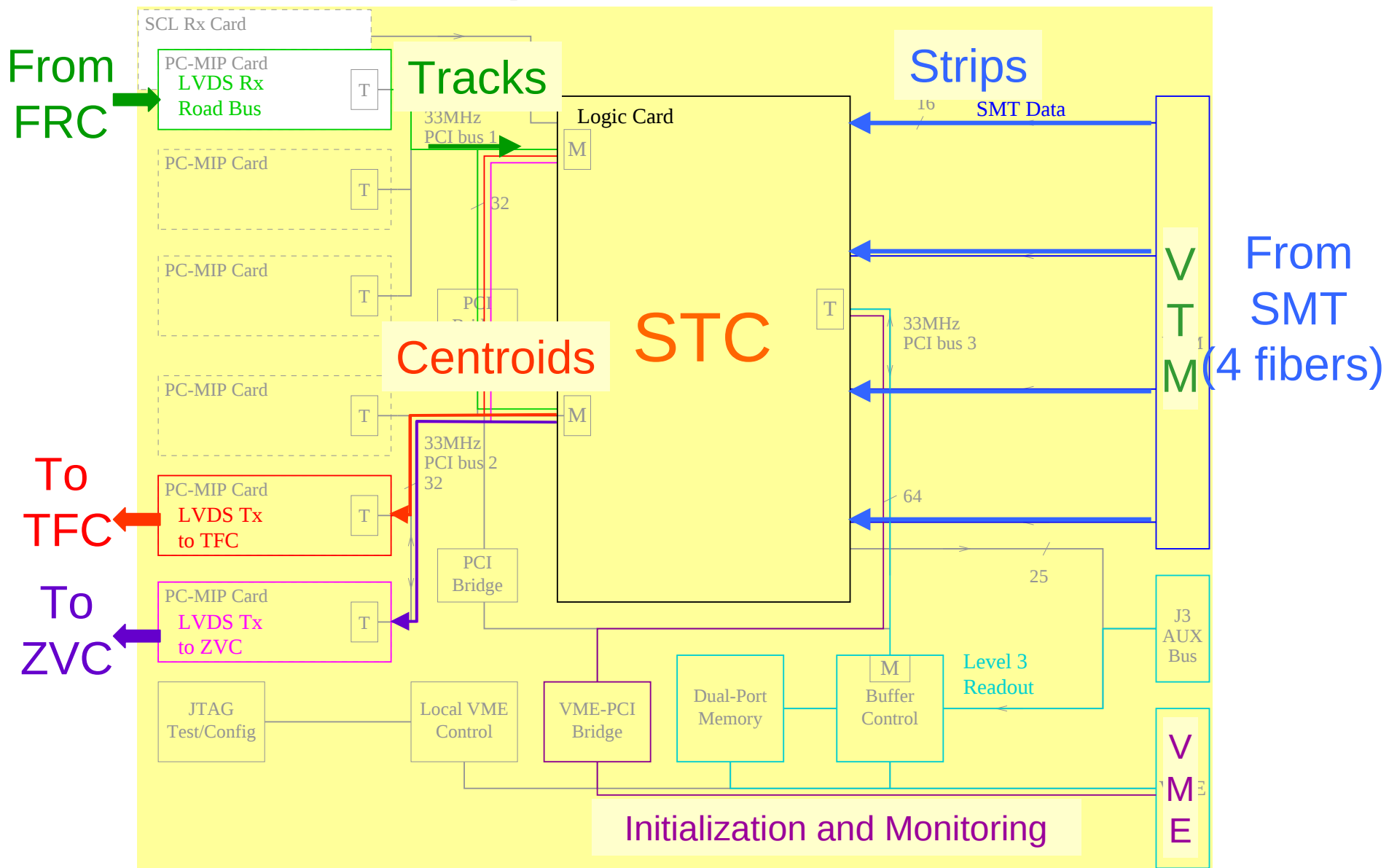
STT crate layout

Six fold STT
symmetry $\Rightarrow$
9 STC cards in
each crate
(72 SMT ladders
on 36 fibers)

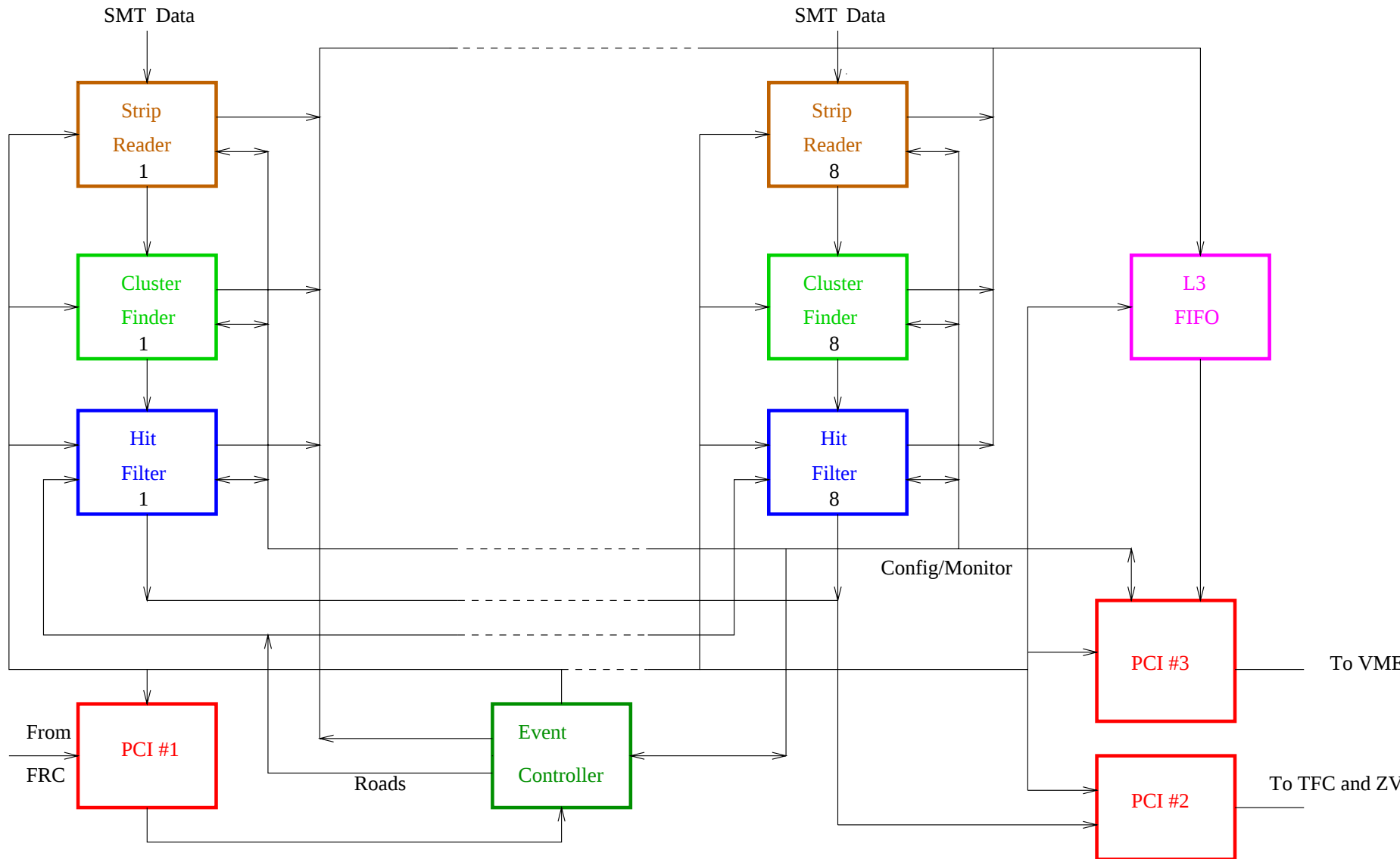


current cabling
scheme suggests
6 out of 36 fiber
will have data
mixed across
30° sectors

Implementation

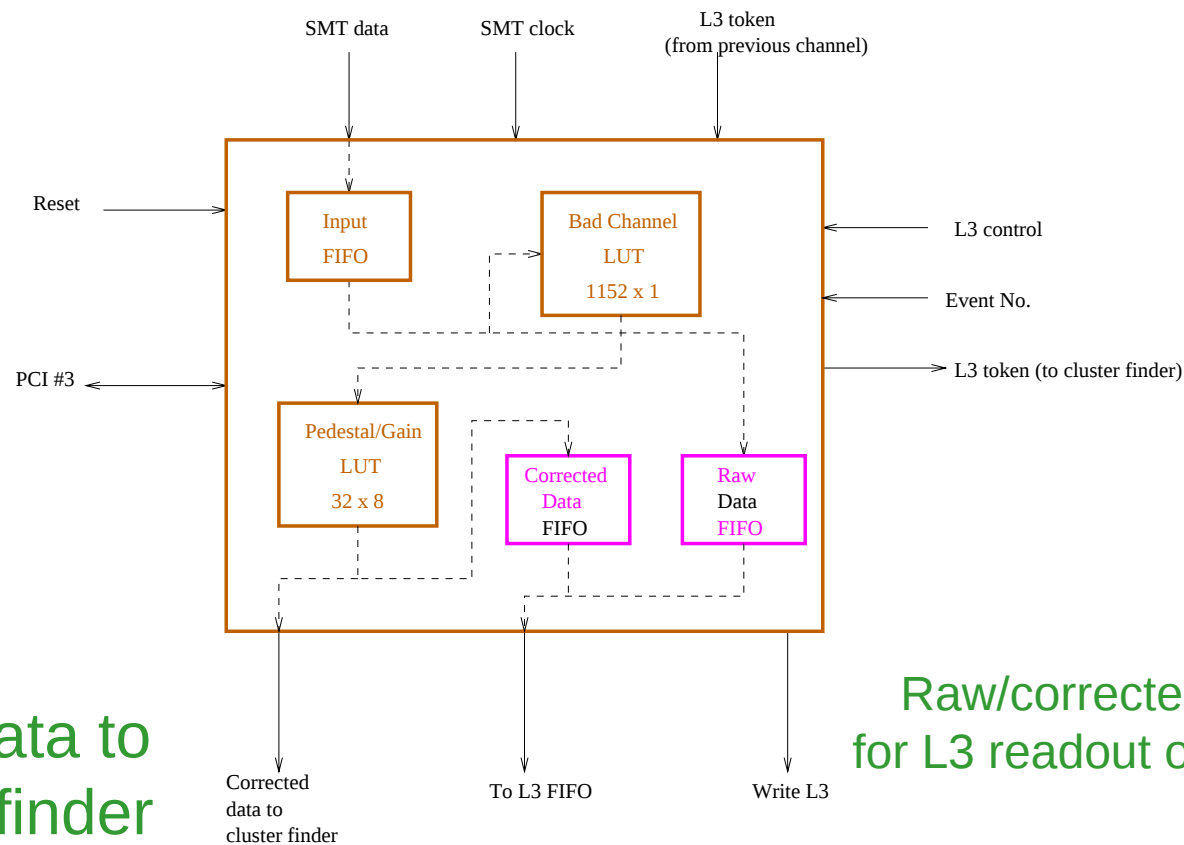


STC Flow Diagram



SMT Data Input Stage

- Read in SMT strip information
- suppress bad channels
- apply gains and pedestal corrections (by chip)

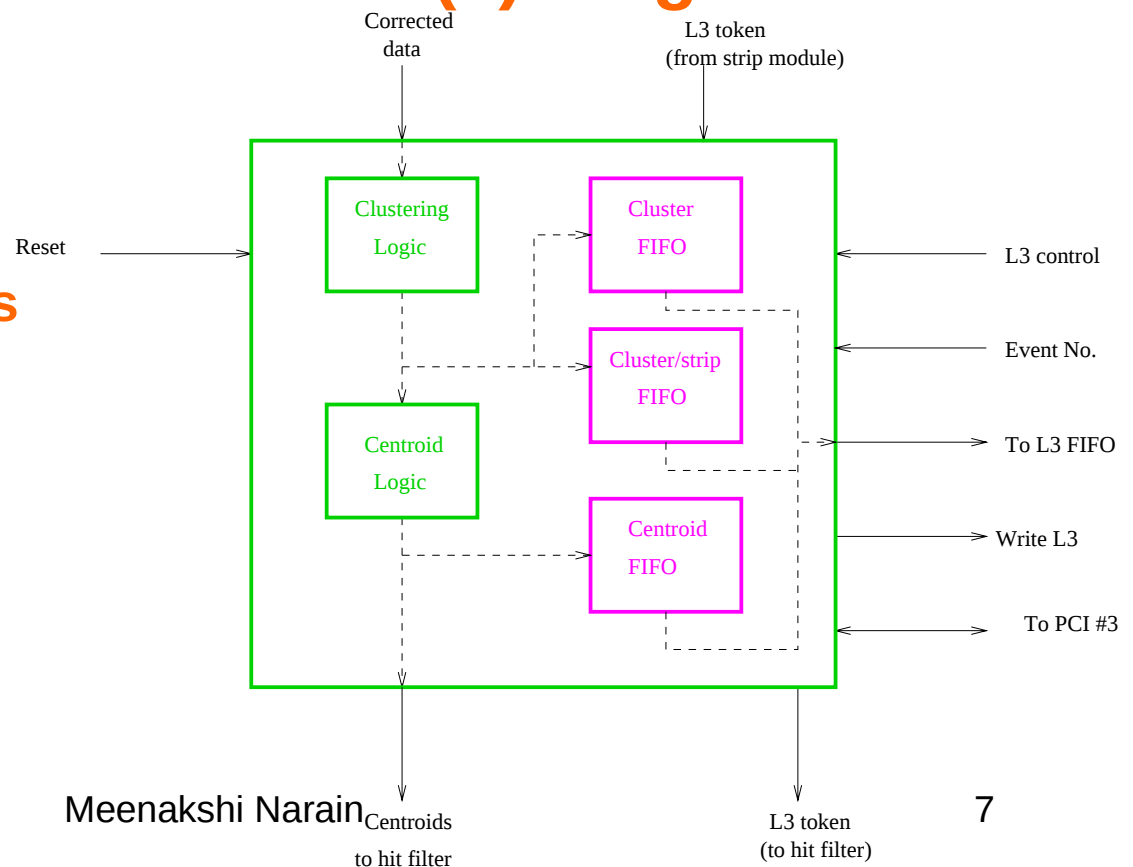


Send data to
cluster finder

Raw/corrected data available
for L3 readout on unbiased events

Clustering Stage

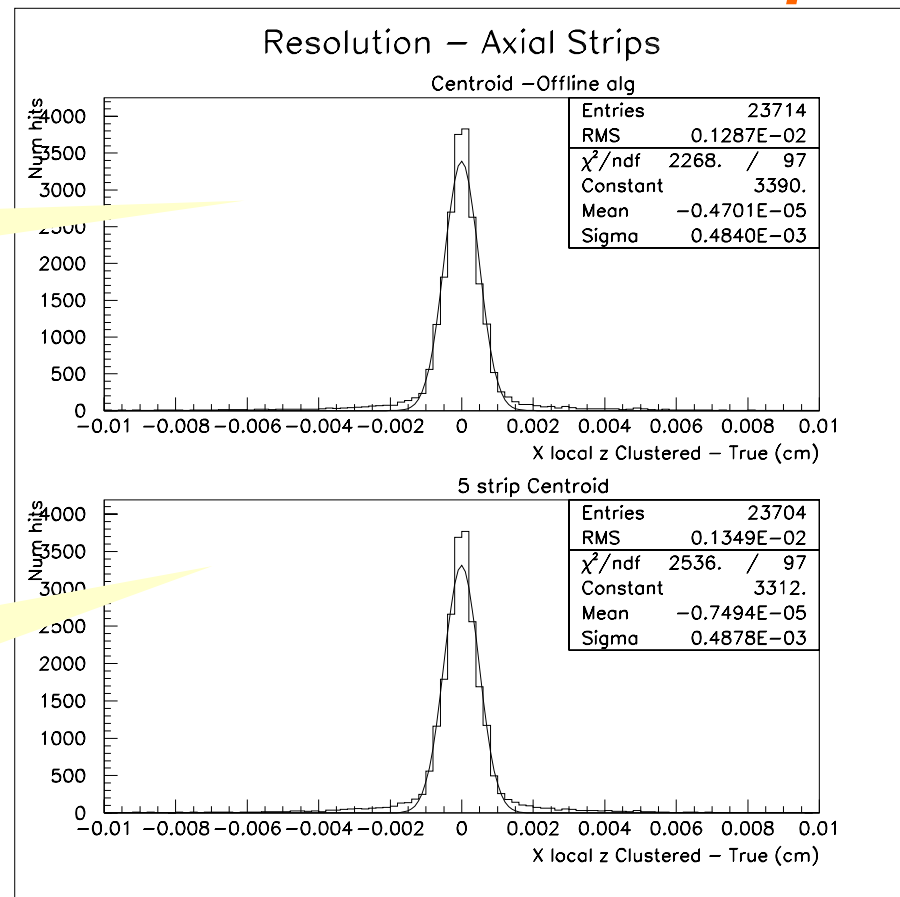
- Combine contiguous strips above a threshold into clusters
 - Compute cluster centroid based on peak with the highest pulse height and its $\pm 2(1)$ neighbours
 - Centroids sent to Hit Filter and L3 FIFO
 - Compute dE/dx thresholds
-
- ```
graph TD; CD[Corrected data] --> CL[Clustering Logic]; L3T[L3 token from strip module] --> CL; CL --> CF[Cluster FIFO]; CF --> L3C[L3 control]; R[Reset] --> CL; CL -.-> CF; CF -.-> CL;
```
- The diagram illustrates the internal logic of the L3 module. It features a central green box containing two main components: 'Clustering Logic' (a green box) and 'Cluster FIFO' (a pink box). 'Corrected data' (indicated by a downward arrow) and an 'L3 token (from strip module)' (indicated by a downward arrow) are inputs to the 'Clustering Logic'. The output of the 'Clustering Logic' is sent to the 'Cluster FIFO' (indicated by a solid arrow). The 'Cluster FIFO' has two feedback paths to the 'Clustering Logic': a dashed arrow pointing right and a dashed arrow pointing left. A 'Reset' signal (indicated by a horizontal arrow) is applied to the 'Clustering Logic'. Finally, the 'Cluster FIFO' outputs an 'L3 control' signal (indicated by a horizontal arrow pointing right).



# Clustering & Centroid Algorithm

- Keep L2STT clustering same as Offline
- Limit centroid calculation to 5 *central strips*

Resolution for  
offline algorithm



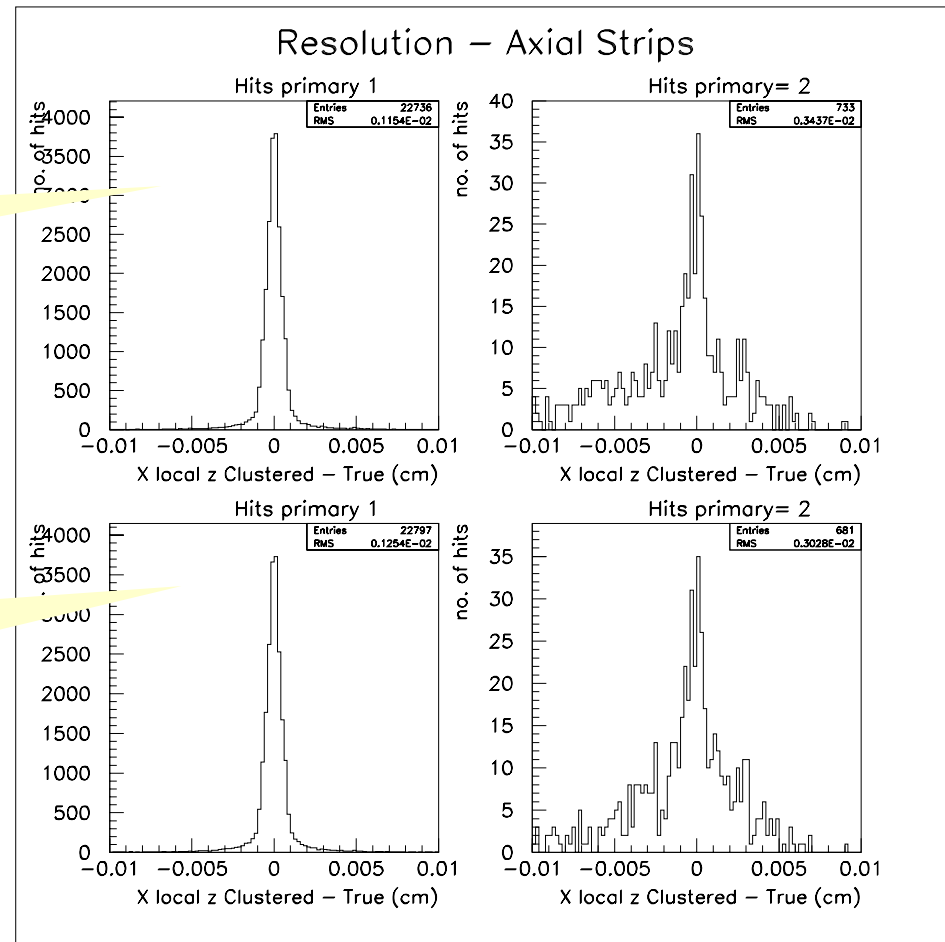
Resolution for  
5 strip centroid algorithm

# Clustering & Centroid Algorithm

- Resolution for clusters with hits from multiple tracks

Resolution for  
offline algorithm

Resolution for  
5 strip centroid algorithm



# Event Controller and Hit Filter

- **Event Controller read in data from FRC**

- **Event information**

- (Evt #, SCL info, Level1 Qualifiers)

- **Read L1CTT tracks**

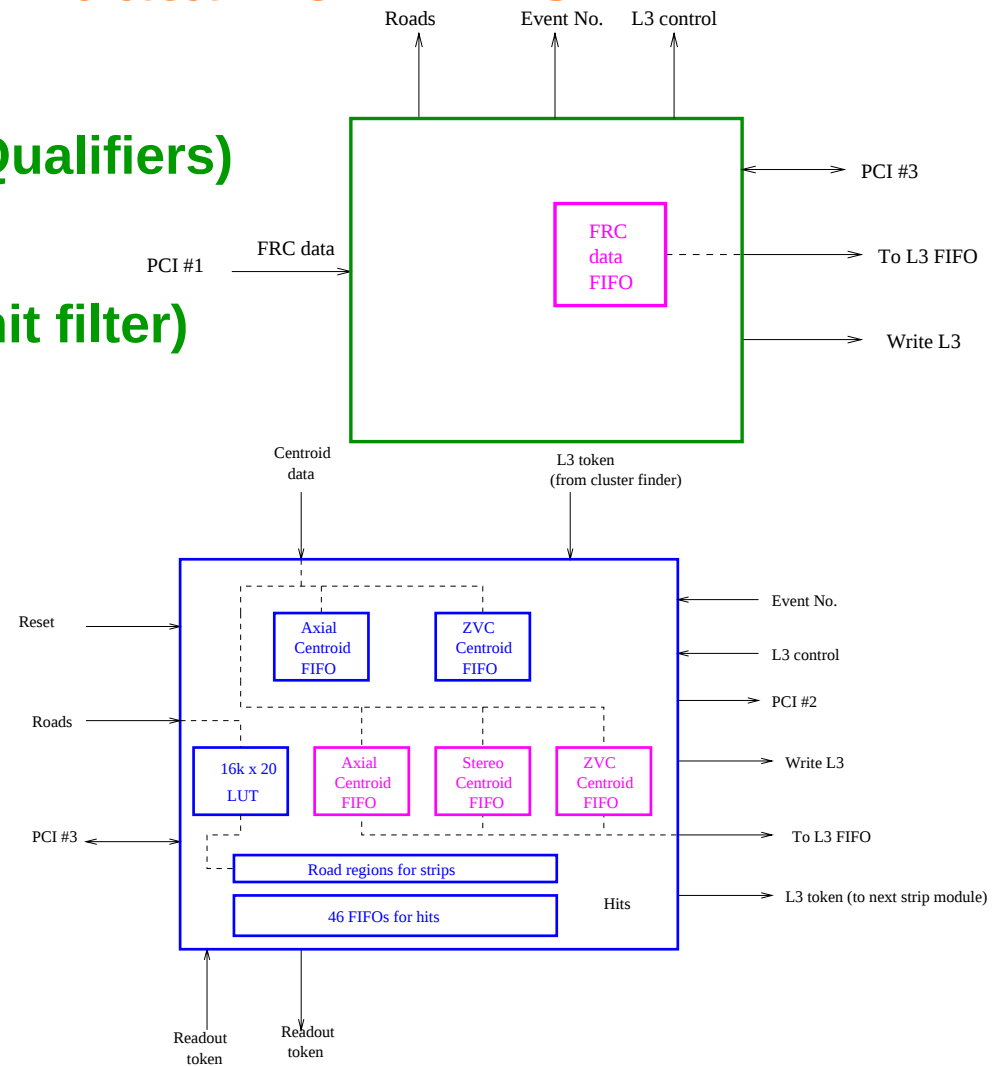
- (send necessary info to hit filter)

- **Hit Filter**

- **convert L1CTT road to SMT roads**

- **collect all centroids in a given road**

- **send centroids in road to TFC**



# Data Output

| Data type                         | L3<br>(normal) | L3<br>(unbiased) | TFC |
|-----------------------------------|----------------|------------------|-----|
| Raw                               |                |                  |     |
| Corrected                         |                | 1 of 8           |     |
| Cluster<br>(incl strips)          |                | 1 of 8           |     |
| Centroids<br>Axial, 2-deg, 90-deg | X              | X                |     |
| Centroids<br>In roads             |                | X                | X   |
| L1CTT info                        |                | X                |     |
| Bytes/event                       | 160            | 630              | 136 |

# Configuration and Monitoring

- **Monitor : (on CollectStatus L1\_QUAL send the following to the CPU)**
  - error counts for all 8 STC channels/card
  - 8-bit histogram of channel hit
  - Total # of axial/ 2°/ 90° centroids for each channel
  - Time spent in various processing states
  - # of hits transferred to TFC
- **Configuration:**
  - look up tables
    - gains, pedestal, road conversion, various thresholds
  - `begin run' download:
    - bad channel list
    - L3 and monitor readout data-type

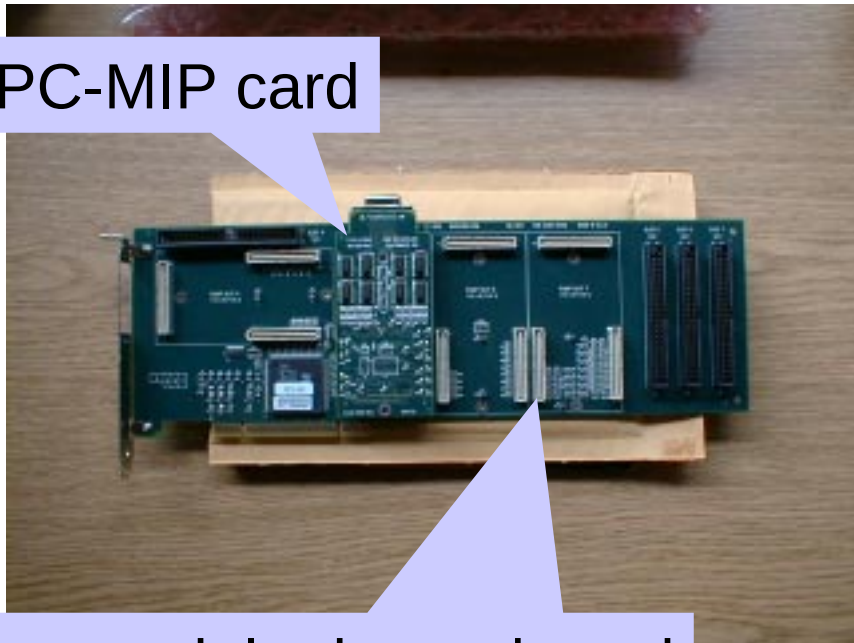
# Functional Simulation

- **clustering algorithm and centroid computation**  
(June'99 version)
  - **Resource allocation for device EPF10K50EQC208-1**
    - **assume: 1 MHz Clock, Single Chip, No bad/skipped channels**

|                            |           |        |
|----------------------------|-----------|--------|
| Total logic cells used:    | 1433/2880 | ( 49%) |
| Total embedded cells used: | 40/160    | ( 25%) |
| Total EABs used:           | 8/10      | ( 80%) |
| Average fan-in:            | 3.24/4    | ( 81%) |
| Total flipflops required:  | 481       |        |
  - **Static Timing Analysis of Baseline Design showed 30MHz Maximum Clock Freq**
  - **Performance limited by Clustering Module.**
  - **Beginning Revision 2 Design...**
    - **Add Hit Filter**
    - **Add 3 or 5 strip cluster finder option**
    - **Examine PCI bus interface**
    - **Add L3 buffer/monitoring requirements.**

# STC development and test platform

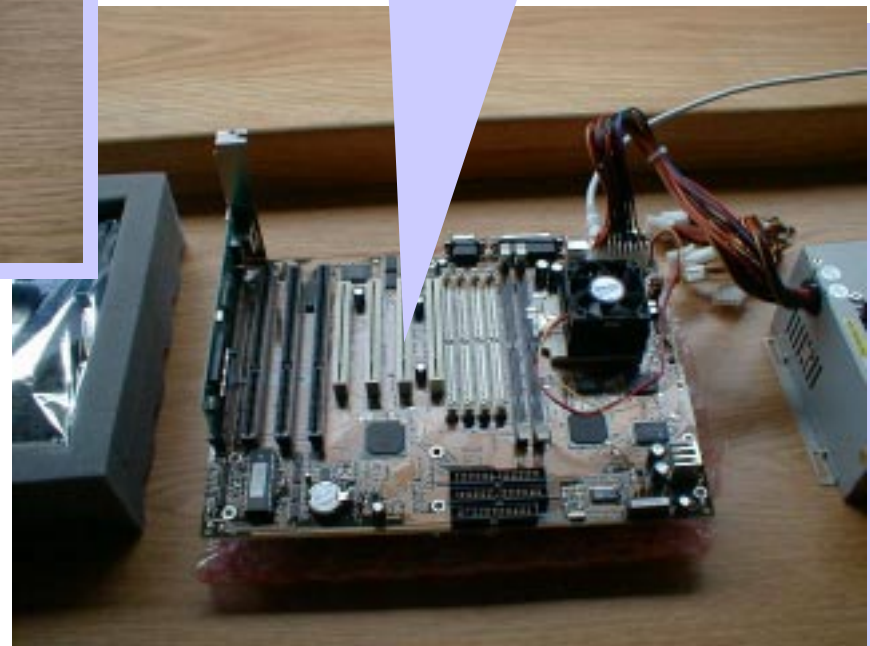
PC-MIP card



commercial adapter board

development platform

PC mother board



# Summary

- **Specifications near completion**
- **Functional simulation started to assess the timing and resources needed**
- **Expect to start layout by 6/1/00**
- **Prototype next fall**