DØnote # ????

# Specifications for the Silicon Trigger Card

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## Contents

# 1 Overview

The Silicon Trigger Card (STC) is a part of the Level-2 Silicon Track Trigger preprocessor (STTpp) [1] for the DØ Upgrade. Figure 1 shows a schematic drawing of the conceptual STTpp design.

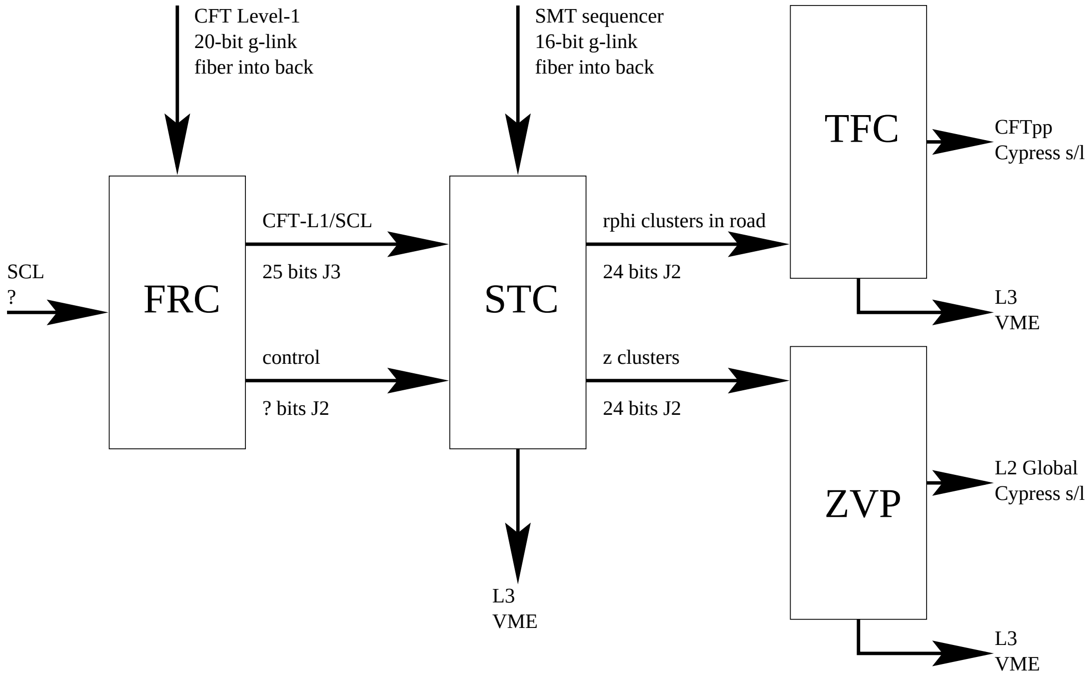


Figure 1: Schematic drawing of the STTpp design.

The STC has to fulfill the following functions:

- receive CFT data from the fiber road card (FRC) and convert them to roads in SMT;
- receive SMT data from sequencers over optical fibers and find hit clusters;
- buffer SMT hit clusters
- select SMT hit clusters that are inside the roads defined by CFT data;
- buffer SMT filtered clusters;
- transmit the $r$-$\phi$ hit clusters in the roads to the track fit cards (TFC);
- transmit the $z$ hit clusters to the z-vertex card (ZVC);
- buffer hit clusters for readout to Level-3 over VME;

# 2 Mechanical Construction

Six VIPA crates accomodate the entire STTpp electronics. Each of these crates serve two SMT sectors, each covering 30° in azimuth. The crates have standard J1 and J2 backplanes, and a custom SVX J3 backplane [2], also used in the VME Readout Buffer (VRB) [3] crates. The slot assignment is defined by the SVX J3 backplane to be

| slot | card |
|---|---|
| 1 – 8 | VBD, TFC, ZVP |
| 9 – 14 | STC |
| 15 | FRC |
| 16 – 21 | STC |

The STC is constructed as a 9U×400 mm VME board. It complies with ANSI/IEEE STD 1014 and VME64 Draft Specifications, Rev. 11.1. Connectors P1 and P2 are 5-row, 160-pin DIN connectors, P3 is a 5-row, 235-pin AMP connector with 2mm pin pitch. There will be 9 or 12 STCs in each STTpp crate, depending on the number of barrel segments in the SMT.

# 3 Data Input and Output

## 3.1 16-Bit G-Link from SVX Sequencer Boards

The SMT data are transmitted over optical fibers 160 ft long from the SVX Sequencer Boards [4] on the detector platform. A passive optical splitter in the movable counting house creates two data paths, one to the VRB for readout to Level-3 and the other to the STTpp. A Hewlett-Packard G-Link transmitter chip formats the data for transmission. Each fiber transmits the data streams from two HDIs, each 8 bits wide. These 16 bits change at a rate of about 53 MHz. For each HDI the data consists of the following sequence of 8-bit words:

$$
\begin{array}{ll}
\left.\begin{array}{l}\text{sequencer ID}\\ \text{HDI ID, status}\end{array}\right\} & \text{header}\\
\left.\begin{array}{l}\text{SVXII chip ID}\\ \text{byte of zeroes}\\ \left.\begin{array}{l}\text{channel ID}\\ \text{data}\end{array}\right\}\begin{array}{l}\text{repeated for}\\ \text{all channels}\end{array}\end{array}\right\} & \begin{array}{l}\text{repeated}\\ \text{for all}\\ \text{SVXII chips}\end{array}\\
\text{hex C0} & \text{trailer}
\end{array} \tag{1}
$$

Each sequencer drives four fibers. These four fibers plug into a G-Link Transition Module (VTM) [5] at the VRB end which holds four HP G-Link decoders. The VTM sits in the rear card cage of the VIPA crate that holds the VRBs. The data are transmitted through the SVX J3 backplane to the VRB[1], sitting in the same slot in the front card cage. The STTpp will use the same arrangement with the VRBs replaced by STCs.

## 3.2 Fiber Road Bus

The CFT Level-1 data are transmitted from the CFT Concentrator Cards on the detector platform via optical cable using HP G-link transmitters and decoders in 20-bit mode. The Fiber Road Card receives and decodes these data and broadcasts them to the STCs over the J3 backplane. The SVX J3 backplane provides a 25 bit bus that connects slot 15, the driver slot in which the FRC sits, with slots 9–14 and 16–21, the receiver slots in which the STCs sit. This bus is connected to pins c1–c25 on the P2 connector. Of the 25 traces, 24 are used for data and one for a strobe.

## 3.3 $r\phi$ Cluster Bus

The $r\phi$ clusters in the CFT roads are transmitted to the Track Fit Card (TFC) over the J2 backplane. The P2 connector has 110 user defined pins (odd numbered pins in row a, b1–32, c1–32, d1–30) [6]. We would like to operate this bus at 40 MHz and it needs to be at least 29 bits wide:

| 29 ... 28 | 27 ... 20 | 19 ... 16 | 15 ... 13 | 12 ... 10 | 9 ... ... ... 1 |
|---|---|---|---|---|---|
| dE/dx | track | sequencer | HDI | chip | strip |

[1]for pinouts see reference [3].

### 3.4 $z$ Cluster Bus

The $z$ clusters are transmitted to the $z$ Vertex Processor (ZVP) over the J2 backplane. This bus is analogous to the $r\phi$ cluster bus in specification, except that it transmits only 17 bits:

| | | | |
|---|---|---|---|
| 17 ... 14 | 13 ... 11 | 10 ... 8 | 7 ... ... ... 1 |
| sequencer | HDI | chip | strip |

### 3.5 Control Lines

The FRC controls the operation of the STTpp crate. Control information is transmitted via the J2 backplane. The information exchanged with the STC consists of buffer pointers, a done flag indicating all SMT data have been received and processed in the STC for a given event, ...

### 3.6 VME readout to Level-3

All hit clusters (with road information?) are read out by a VBD over VME when an event is accepted by Level-2.

# 4 Functional Description

The STC has eight identical data channels, corresponding to the eight HDI data streams it receives from the SMT. Figure 2 shows a block diagram of one STC channel.

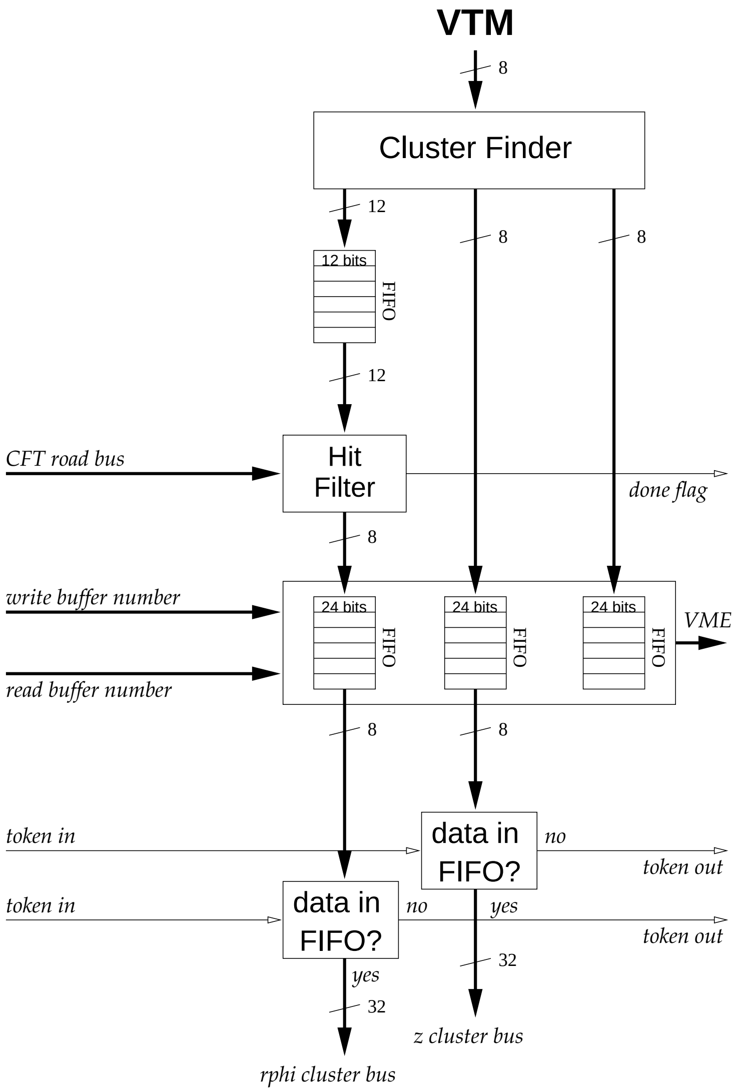


Figure 2: Block diagram of one STC channel.

# 5 Input from SMT Front-Ends

Optical fibers transmit the SMT data from the front-ends to the VRB cards in the counting house. The data from each silicon detector consists of alternating 8-bit address and signal words. The data from two silicon detectors are transmitted over each fiber at a rate of 106 Mbyte/s. Passive splitters in the fibers create a data path into the L2STT, where the fibers plug into the same VME transition module (VTM) as used for the VRBs. The data are loaded into a FIFO as they are received.

Digitizing the SVXII data takes about 3 $\mu$s and there is an additional small latency of about 100 ns from the cluster finding. Thus the SMT data arrive in the FIFO at the output of the cluster finder roughly at the time the roads are set up. Every fiber carries data from about 2000 SMT channels. Monte Carlo simulations predict an average of 40 hits per fiber, corresponding to an occupancy of 2% [7] and a maximum of 180

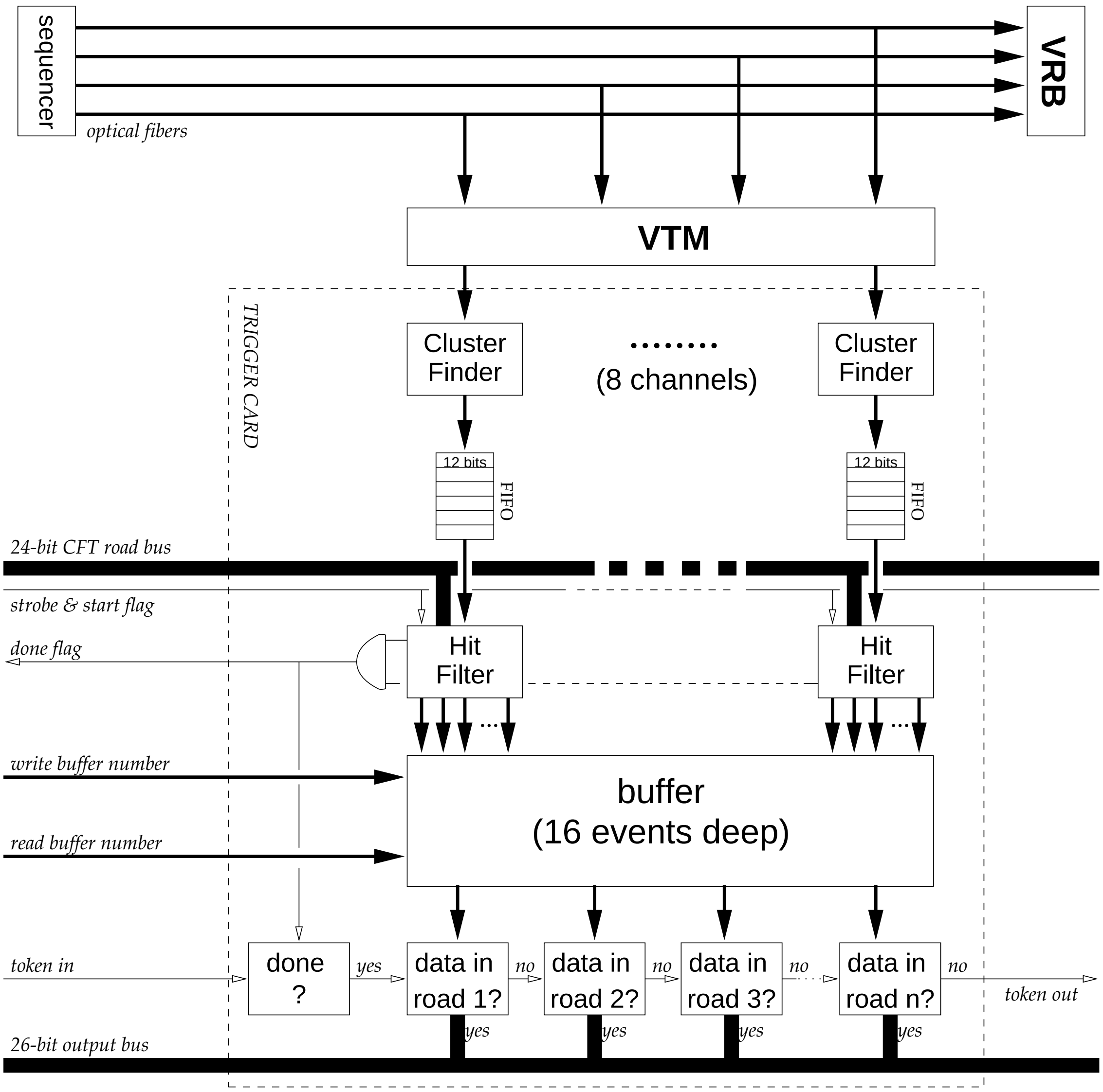


Figure 3: Block diagram of trigger card.

hits per fiber. We add 1% occupancy from noise (see analysis of test beam data [8]). We thus have 60–200 channels to read out. At 53 MHz this will take 1.1–3.8 $\mu$s.

The L2STT has to provide seamless coverage of all barrel segments that belong to one SMT sector covering 30° in azimuth, because many tracks cross from one barrel section into another. Very few tracks are not contained in a single SMT sector[7]) so that each sector can be treated as an independent unit. This means that the data from all barrel segments of any one SMT sector must be routed to the same L2STT crate. In the six barrel sections, there are 36 detectors per sector. Each VTM accepts four fibers and each fiber carries the data from two detectors so that each trigger card has eight identical channels, each processing the data from one detector. We can therefore accommodate two SMT sectors in an L2STT crate that is populated with nine trigger cards.

# 6 Hit Finding

An FPGA processes the data further. It corrects for pedestals and gains and supresses noisy strips based on a lookup table. It supresses all strips with pulseheights below a threshold. It has to be determined whether these operations need to be performed on a strip-to-strip, chip-to-chip, or global scale. The FPGA then scans the corrected pulseheights for local maxima, *i.e.* strips with larger pulseheights than their two neighbors. Each such local maximum forms the seed for a hit cluster. The position of the hit cluster is determined from a pulseheight averaged center of gravity of up to five adjacent strips, centered on a seed strip, using the following algorithm. Hit clusters cannot extend across two detectors nor can they extend over both sides of a double sided detector.

Let $p_i$ be the 8-bit pulseheight measurement in strip $i$. The strip index $i$ is defined relative to the strip with the local maximum, which has $i = 0$. The 7-bit strip number is $x_i$. Compute

$$n = 8 \times \sum_{i=-2}^{2} p_i i \text{ and} \tag{2}$$

$$m = \sum_{i=-2}^{2} p_i. \tag{3}$$

Then set the offset $\Delta x$ using the following comparisons

$$\begin{array}{rcll} & n & > 5m & \Rightarrow \Delta x = 3/4, \\ 5m > & n & > 3m & \Rightarrow \Delta x = 1/2, \\ 3m > & n & > m & \Rightarrow \Delta x = 1/4, \\ m > & n & > -m & \Rightarrow \Delta x = 0, \\ -m > & n & > -3m & \Rightarrow \Delta x = -1/4, \\ -3m > & n & > -5m & \Rightarrow \Delta x = -1/2, \\ -5m > & n & & \Rightarrow \Delta x = -3/4. \end{array} \tag{4}$$

The cluster centroid is then given to a precision of 1/4 strip pitch by

$$\overline{x} = x_0 + \Delta x. \tag{5}$$

This algorithm avoids floating point divisions which are difficult to implement in an FPGA.

The hit finding runs synchronously with the incoming data so that it introduces only a small latency ($\ll 1$ $\mu$s). The cluster outputs 15 bits: the seven bits used to identify the strip number plus an additional two added by the cluster finding algorithm, three bits to label the eight chips that read out the axial strips or the seven chips that read out the stereo strips, one bit to indicate whether the cluster is on the axial or the stereo side, and 2 bits containing pulse height threshold information. (see figure 4).

Based on bit 13 the clusters are stored in two FIFOs. Only clusters from the axial strips participate in the track finding. The axial strips are read out by the first (last?) three chips for layers 1,2,5, and 6, and by the first (last?) five chips for layers 3,4,7, and 8. The clusters from the axial strips are stored in one FIFO, the clusters from the stereo strips are stored in the other FIFO. All clusters are buffered for readout to Level-3 over the VME bus (?).

| 15 14 | 13 | 12 11 10 | 9 8 7 6 5 4 3 2 1 |
|---|---|---|---|
| dE/dx thr | axial stereo | chip | strip |

Figure 4: Bit allocation in output of cluster finder.

## 6.1 Input from Fiber Road Card

The data from the CFT Level-1 trigger are transmitted from the fiber road card over a bus on the backplane. For every CFT track 24 bits have to be transmitted: 16 bits to identify the inner- and outermost hit fibers and an 8-bit track number. The bus requires 24 signal lines and one strobe line. It runs at 25 ns per cycle. According to Monte Carlo simulations [7], we expect on average less than two CFT tracks per STTpp crate. The maximum number of tracks expected is 25, the maximum number llowed per STTpp crate is 32. It therefore takes on average 50 ns and at most 800 ns to transmit the CFT data across the backplane to the trigger cards. In addition, it takes about 2.4 $\mu$s after a Level-1 trigger accept for the CFT data to arrive at the fiber road cards. That means the road addresses are latched in the trigger cards no later than 3.2 $\mu$s after a Level-1 trigger is accepted.

## 6.2 Conversion of CFT Tracks to SMT Roads

The 16 lines that identify the CFT track address a lookup memory. The output of the lookup memory is a range of strip numbers, consisting of 10 bits each (corresponding to bits 3–12 in figure 4) for the first and last strips. If a track does not go through a detector the corresponding lookup memory will return zero for both strip numbers. Since every input fiber carries the data from two barrel detectors, up to eight strip number ranges have to be determined for every CFT track. Tracks that go through an SMT sector of 60° in azimuth can hit any one of 773 outer fibers. For each outer fiber there are 28 inner fibers that can be hit. So there are 21644 possible CFT tracks for a 60° SMT sector. We therefore need either one lookup memory of 433 kB with 16 address lines and 160 output lines or eight lookup memories of 54 kB each with 16 address lines and 20 output lines. The coordinate conversion can then be performed "on the fly" just like the cluster finding and no time is lost.

### 6.2.1 Road Definition

The fiber hits in the inner and outer CFT layers define a family of tracks, which all go through these fibers. The envelope of all these tracks defines the road in the SMT. For radial positions smaller than that of the inner hit fiber, the tracks with the smallest and largest curvature define this envelope. Figure 5 shows the road in the SMT spanned by two hit fibers in the CFT. The solid lines indicate the road for tracks that pass through the origin. If we also want to accept all hits from tracks with finite impact parameters $b$ the road widens as indicated by the dashed lines.

Figure 6 shows the width of the road in azimuth around the track, defined by the centers of the inner and outer fibers and the origin, versus radius. The black region is the road defined by the envelope of all tracks passing through the origin, the dark shaded region is the road defined by tracks with impact parameter $|b| < 1$ mm, and the light shaded region for $|b| < 2$ mm. Figure 7 shows the road widths in arclength. Table 1 lists the road widths at the mean radii of the silicon layers. In the table "a" and "b" refer to the two overlapping sublayers that make up one silicon layer.

## 6.3 Hit Filter

As the cluster data appear at the output of the cluster-position FIFO, they are processed by a second FPGA. This FPGA simultaneously compares the cluster positions to the upper and lower limits of the all address ranges for all roads. Bits 3–12 in figure 4 are compared to the road limits. Since there can be up to 32 roads and two address ranges per road, 64 10-bit comparators are required per channel. This hit filtering process

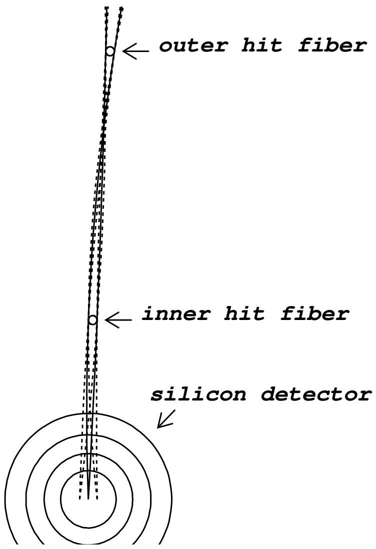


Figure 5: Road definition in the silicon detector.

Table 1: Road sizes in silicon detector.

| layer | radius | road for $b = 0$ | | road for $\|b\| < 1$ mm | | road for $\|b\| < 2$ mm | |
|---|---|---|---|---|---|---|---|
| | | mrad | mm | mrad | mm | mrad | mm |
| 1a | 2.72 cm | $\pm$ 4.2 | $\pm$0.12 | $\pm$34.3 | $\pm$0.93 | $\pm$64.4 | $\pm$1.75 |
| 1b | 3.65 cm | $\pm$ 4.1 | $\pm$0.15 | $\pm$24.8 | $\pm$0.91 | $\pm$45.7 | $\pm$1.66 |
| 2a | 4.55 cm | $\pm$ 4.0 | $\pm$0.18 | $\pm$19.4 | $\pm$0.88 | $\pm$34.8 | $\pm$1.58 |
| 2b | 5.55 cm | $\pm$ 3.9 | $\pm$0.22 | $\pm$15.4 | $\pm$0.86 | $\pm$27.0 | $\pm$1.50 |
| 3a | 6.77 cm | $\pm$ 3.8 | $\pm$0.26 | $\pm$12.1 | $\pm$0.82 | $\pm$20.6 | $\pm$1.39 |
| 3b | 7.58 cm | $\pm$ 3.7 | $\pm$0.28 | $\pm$10.5 | $\pm$0.80 | $\pm$17.5 | $\pm$1.33 |
| 4a | 9.10 cm | $\pm$ 3.6 | $\pm$0.32 | $\pm$ 8.4 | $\pm$0.76 | $\pm$13.2 | $\pm$1.20 |
| 4b | 10.05 cm | $\pm$ 3.4 | $\pm$0.35 | $\pm$ 7.3 | $\pm$0.73 | $\pm$11.2 | $\pm$1.13 |

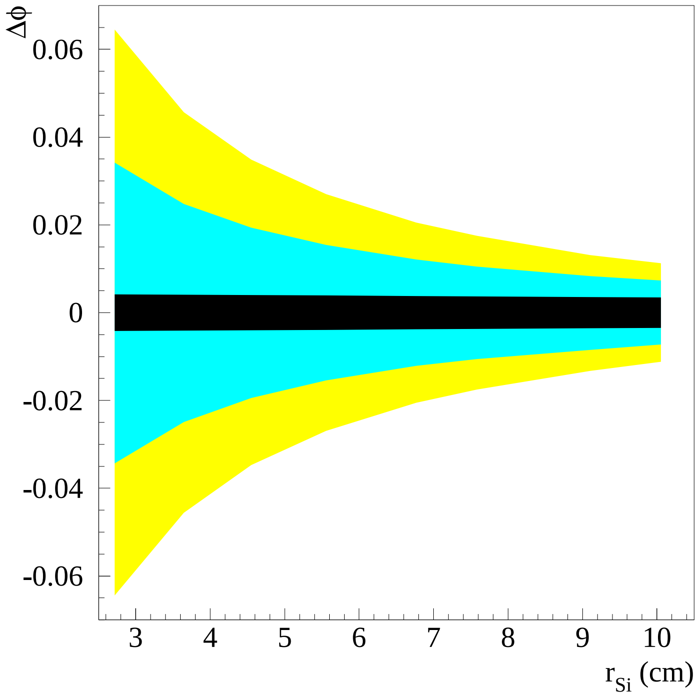


Figure 6: Width of silicon roads versus radius.

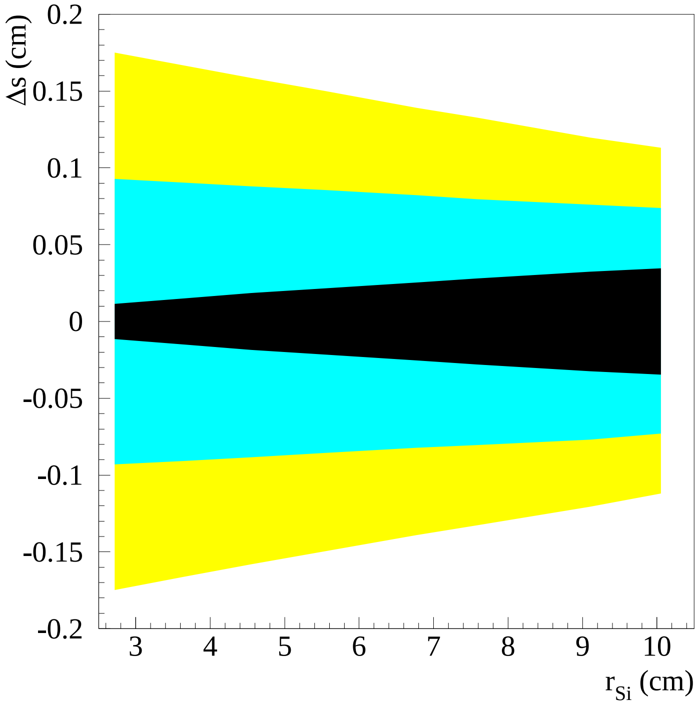


Figure 7: Width of silicon roads versus radius

is performed as the SMT data arrive and will keep up with the data so that it does not cause deadtime but only a small delay equal to the time it takes to process one cluster ($\ll 1\ \mu$s). Figure 8 shows a block diagram of the hit filter FPGA.

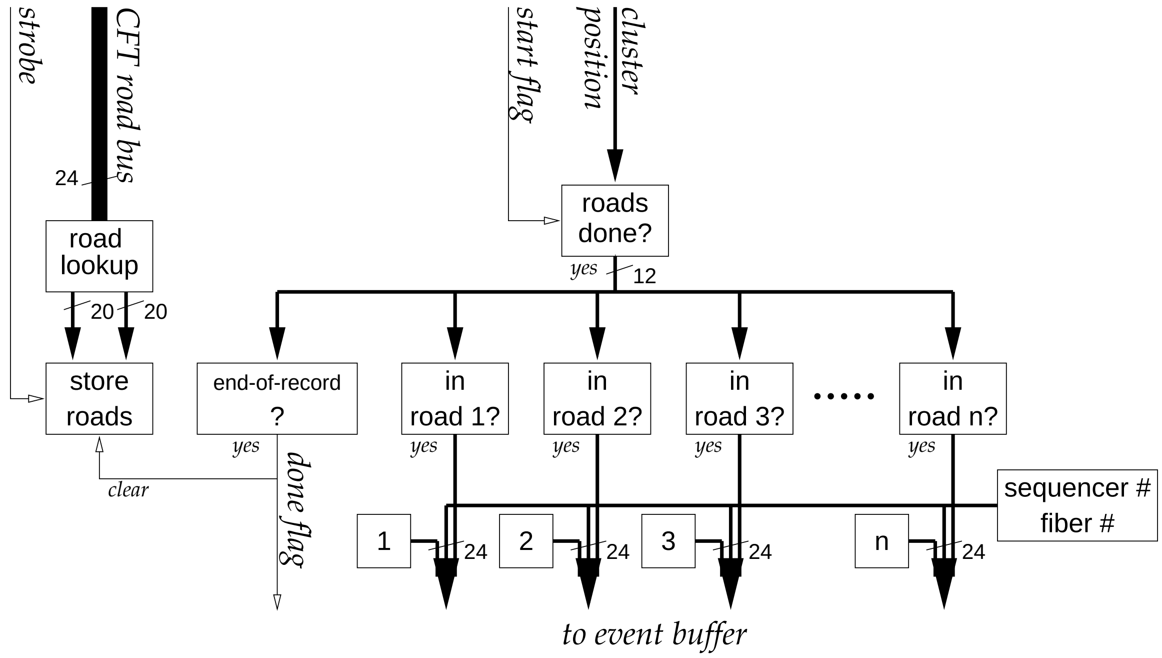


Figure 8: Block diagram of hit filter FPGA.

## 6.4 Event Buffering

The output of the hit finder FPGA is stored in a buffer 16 events deep. There is a FIFO for every road that stores all (12-bit) cluster positions that are inside an address range for this road. An end-of-record code is passed through the cluster finder unaltered. When it appears at the hit filter, it sets a “done” flag to indicate that all data from the fiber has been processed through the cluster finder and the hit filter and has been loaded into a buffer. The logical “and” of the flags from the four hit filters on a trigger card indicates that the trigger card has finished loading an event. The logical “and” of the “done” flags from all trigger cards is formed on the backplane (?) and signals to the fiber road card that an event has been completely loaded into the buffer. The fiber road card then updates the buffer pointer for the next event to point to an empty buffer. At this time the STTpp is ready to accept another event.

## 6.5 Timing

It takes about 2.4 $\mu$s after a Level-1 trigger accept for the CFT data to arrive at the fiber road cards. Bus transfer to the trigger cards takes another 0.8 $\mu$s. That means 3.2 $\mu$s after a Level-1 trigger accept the road addresses are latched on the trigger cards.

Digitizing the SVX-II data takes a little under 3 $\mu$s and there is an additional small latency of about 100 ns from the cluster finding. Thus the SMT data arrive in the FIFO at the output of the cluster finder roughly at the time the roads are set up.

Every fiber carries data from about 2000 SMT channels. Monte Carlo simulations predict an average of 40 hits per fiber, corresponding to an occupancy of 2% [7] and a maximum of 180 hits per fiber. We add 1% occupancy from noise (see analysis of test beam data [8]). We thus have 60–200 channels to read out. At 53 MHz this will take 2.3–7.6 $\mu$s. Only half the hits (from the axial strips) form clusters and the reduction from number of hits to number of clusters should be about a factor two. Thus there will be 15–50 clusters which have to be compared to the strip ranges that define the roads. The comparisons for all roads are performed in parallel. For each road there is a FIFO and a cluster that is in the strip range for a road is stored in the corresponding FIFO. This should not take longer than 100 ns (?) per cluster, *i.e.* 1.5–5.0 $\mu$s. This is less time than required for the readout of the SMT. The cluster filtering can therefore effectively be performed without latency.

All hit clusters in the roads for an event are loaded into a buffer about 5. 5–10.8 $\mu$s after the Level-1 trigger accepted the event, but not later than completion of the readout of the SMT data. At this time the STTpp is ready to accept another event from Level-1.

## 6.6 Transfer of Hits to Processor Card

For each hit 29 bits need to be transferred: 7+2 bits for the fractional strip number, 3 bits to identify the chip #, 3 bits to specify the HDI within a sequncer, 4 bits to identify the sequencer, a 8-bit track number, and a 2-bit dE/dx threshold (figure 9). The lower 12 bits are the same as at the output of the cluster finder (figure 4).

| 29 ... 28 | 27 ... 20 | 19 ... 16 | 15 ... 13 | 12 ... 10 | 9 ... ... ... 1 |
|---|---|---|---|---|---|
| dE/dx | track | sequencer | HDI | chip | strip |

Figure 9: Bit allocation in output to processor card.

The data transfer occurs over a dedicated backplane bus which provides unidirectional, data-driven broadcast from the trigger cards to the track fit card. It is initiated by the presence of data in the event buffer. The first trigger card transmits the lists for all roads over a 26-bit bus to the track fit card. For each road the first record consists of the CFT data and the road number. These are the 24 bits sent from the fiber road card to the trigger cards. Then all hits in the road are transferred. This sequence is repeated for all roads. When the card has finished transmitting the list it passes a token to the next trigger card and so on until all trigger cards that serve the same azimuthal sector in the SMT have transmitted their data to the track fit card.

There are on average 42 and at most about 500 clusters in all roads of an L2STT crate [7]. If the bus operates at 25 ns/cycle, the transmission of these clusters and the CFT data to the track fit card will take on average 1.1 $\mu$s and at most 13.3 $\mu$s.

## 6.7 VME Interface

### 6.7.1 Parameter Download

The VME interface has to support the download of the lookup tables for the conversion of CFT coordinates to address ranges in the SMT for the roads, and

### 6.7.2 Diagnostics

In mark-and-pass mode all cluster and road information is transmitted to Level-3 over the VME bus and a VRB.

# References

[1] H. Evans *et al.*, “A Silicon Track Trigger for the DØ Experiment in Run II”, `http://www-d0.fnal.gov/ heintz/public_html/d0_private/tdr_12.ps`.

[2] J. T. Anderson, K. Woodbury, ESE-SVX-960130, `http://www-ese.fnal.gov/eseproj/svx/j3_bkpln/j3_bkpln.html`

[3] `http://www-ese.fnal.gov/eseproj/svx/vrb/vrb.pdf`.

[4] M. Utes, DØ engineering note 3823.110-EN-480.

[5] reference for VTM receiver module.

[6] VME64, VME64x.

[7] "Dataflow Requirements for the Silicon Track Trigger", DØ note ????, M. Narain, 1998.
The expected averages are based on an average of 4 interactions/crossing, corresponding to $\mathcal{L} = 2 \times 10^{32}$ cm$^{-2}$s$^{-1}$ and a crossing interval of 396 ns. The expected maximum is based on the endpoint of the spectra for 8 interactions.

[8] `http://d0sgi0.fnal.gov/řoco/vertex/tbtalk.ps`