MEMORY MAP for the STC LOGIC DESIGN

Alexandre ZABI and Shouxiang Wu

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Abstract

This paper gives the memory map for the STC. All addresses used to download data into the STC logic design are specified.

1 STC

This table shows the PCI3 address for the STC memory blocks:

Memory	PCI-Address[17-0]	size
Road memory	0x00000	64 kbytes
L3 memory	0x10000	64 kbytes
Control Logic	0x20000	64 kbytes
Channel Logic	0x30000	64 kbytes

1.1 STC CHANNELS

STC CHANNEL SELECTION:

When the Channel-Logic memory space is selected, the bits 15 to 13 of the PCI3 address are used to specify the STC-Channel logic.

Channel-select = PCI-address(15 downto 13).

STC CHANNEL	PCI-Address(15 downto 13)
Channel 0	000
Channel 1	001
Channel 2	010
Channel 3	011
Channel 4	100
Channel 5	101
Channel 6	110
Channel 7	111

STC CHANNEL MEMORY SPECIFICATIONS:

Once a STC channel has been selected, the internal memories of that particular channel can be accessed. The addresses of these memories appear in the following table.

STC memory select = PCI-address(12 downto 0).

MEMORY	PCI-Address[12-0]	SIZE(bytes)
Monitor	1B00	128 bytes
Miscellaneous	1A00	256 bytes
Bad Channel	1800	288 bytes
Test LUT	1000	2032 bytes
Gain Offset	0000	2304 bytes

MEMORY SPACE SPECIFICATION:

This part gives the addresses to download parameters into the STC memory blocks.
The memory status are the following:

- R ⇒ READ ONLY
- W ⇒ WRITE ONLY
- R/W ⇒ READ/WRITE.
- MONITOR:

  The Monitor is a READ ONLY memory. It implements a set of 16, 32-bit counters to keep track of errors flags, number of strip active per chip, number of centroids etc. After latching the MONITOR, the results of those counters get registered and can be accessed through PCI3 using the following addresses:

PCI-Address[12-0]	SIZE	DESCRIPTION	BIT USED	MEM STATUS
0x1B00	4 bytes	Nbr of strips for chip0	31-0	R
0x1B04	4 bytes	Nbr of strips for chip1	31-0	R
0x1B08	4 bytes	Nbr of strips for chip2	31-0	R
0x1B0C	4 bytes	Nbr of strips for chip3	31-0	R
0x1B10	4 bytes	Nbr of strips for chip4	31-0	R
0x1B14	4 bytes	Nbr of strips for chip5	31-0	R
0x1B18	4 bytes	Nbr of strips for chip6	31-0	R
0x1B1C	4 bytes	Nbr of strips for chip7	31-0	R
0x1B20	4 bytes	Nbr of strips for chip8	31-0	R
0x1B24	4 bytes	Nbr of Smt data with Vtm-error bit set	31-0	R
0x1B28	4 bytes	Nbr of Seq or Hdi Mismatch	31-0	R
0x1B2C	4 bytes	Nbr of Zero byte missing after Chip id or Chipid Msb not set	31-0	R
0x1B30	4 bytes	Nbr of Undefined Centroids	31-0	R
0x1B34	4 bytes	Nbr of Stereo centroids	31-0	R
0x1B38	4 bytes	Nbr of Axial centroids	31-0	R
0x1B3C	4 bytes	Nbr of 90 degrees centroids	31-0	R

- MISCELLANEOUS:

The miscellaneous is a memory space used to store the parameters needed by the Channel logic. These parameters and the associated memory spaces are given in this table.

MEMORY	PCI-Address[12-0]	Size
Seq-hdi-parameter	0x1AA0	8 bytes
Threshold	0x1A80	32 bytes
Data-Type	0x1A40	64 bytes
Pulse-Area	0x1A00	64 bytes

DESCRIPTION OF THE MISCELLANEOUS MEMORIES:

SEQUENCER-HDI:

One SEQUENCER-ID and one HDI-ID must be downloaded in the SEQ-HDI memory. These parameters are also used by the L3-EVENT-BUILDER.
Thus there are written into mirror registers. These are READ ONLY and use the same addresses but different bit locations.

SEQ-HDI				
PCI-ADDRESS[12-0]	SIZE	PARAMETERS	BIT USED	MEM status
0x1AA4	4 bytes	Seq-id (8-bit) Seq-id(8-bit) from mirror in l3 event builder	7-0 23-16	R/W R
0x1AA0	4 bytes	Hdi-id (3-bit) Hdi-id(3-bit) from mirror in l3 event builder	2-0 18-16	R/W R

DATA-TYPE:

The Data Type memory is used to store the 2-bit DATA-TYPE associated to each SVXII chip mounted on a ladder. Each Silicon detector has either axial and 90 degrees strips or axial and stereo strips. The DATA-TYPE is encoded as following:

- 00 ⇒ undefined (illegal chip-id)
- 01 ⇒ Stereo
- 10 ⇒ Axial
- 11 ⇒ Z

There are up to 9 SVXII chips on a ladder. They are identified with a 4-bit CHIP-ID word that is used to access the DATA-TYPE memory. A CHIP-ID that would return a 00 DATA-TYPE is considered illegal. The data from the associated strips would be discared unless the ACCEPT-BAD-CHIP signal is set in the RUN-CTL register of the CONTROL-LOGIC. Another 1-bit parameter is stored in the CONTROL-LOGIC as data are being downloaded into the DATA-TYPE memory. This bit indicates whether the STC channel selected receives data from stereo or 90 degrees strips. When this bit is set to 1, the STC channel receives data from 90 degrees Strips. This bit can be checked as reading Data-Type from a particular Channel and it is located as bit 15.

DATA-TYPE				
PCI-ADDRESS[12-0]	SIZE	PARAMETER	BIT USED	MEM status
0x1A40	4 bytes	data-type (2-bit) ⇒ for chip0	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A44	4 bytes	data-type (2-bit) ⇒ for chip1	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A48	4 bytes	data-type (2-bit) ⇒ for chip2	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A4C	4 bytes	data-type (2-bit) ⇒ for chip3	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A50	4 bytes	data-type (2-bit) ⇒ for chip4	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A54	4 bytes	data-type (2-bit) ⇒ for chip5	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A58	4 bytes	data-type (2-bit) ⇒ for chip6	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A5C	4 bytes	data-type (2-bit) ⇒ for chip7	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A60	4 bytes	data-type (2-bit) ⇒ for chip8	1-0	R/W
		Z or Stereo data (1-bit)	15	R
0x1A64	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A68	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A6C	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A70	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A74	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A78	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W
0x1A7C	4 bytes	00 ⇒ (illegal chip id)	1-0	R/W

THRESHOLD:

The threshold LUT stores the thresholds used in the clustering algorithm. There are two thresholds for each type of strips (Theshold2 > Threshold1). These thresholds may also be read out from the mirrors located in the CONTROL-LOGIC. The mirrors must show the same threshold values when reading back from the THRESHOLD memory.

THRESHOLD				
PCI-Address[12-0]	SIZE	DESCRIPTION	BIT USED	MEM status
0x1A80	4 bytes	not used		
0x1A84	4 bytes	not used		
0x1A88	4 bytes	stereo-threshold1(8-bit) from mirror(8-bit)	7-0 23-16	R/W R
0x1A8C	4 bytes	stereo-threshold2(8-bit) from mirror(8-bit)	7-0 23-16	R/W R
0x1A90	4 bytes	axial-threshold1(8-bit) from mirror(8-bit)	7-0 23-16	R/W R
0x1A94	4 bytes	axial-threshold2(8-bit) from mirror(8-bit)	7-0 23-16	R/W R
0x1A98	4 bytes	z-threshold1(8-bit) from mirror(8-bit)	7-0 23-16	R/W R
0x1A9C	4 bytes	z-threshold2(8-bit) from mirror(8-bit)	7-0 23-16	R/W R

PULSE-AREA:

The PULSE-AREA memory stores the thresholds used to evaluate the pulse height of the cluster. The total energy of the cluster is compared with the 7, 11-bit thresholds to generate the 3-bit PULSE-AREA. Because each STC channel processes two types of strip data, there are 14 thresholds overall.

PULSE-AREA				
PCI-Address[12-0]	SIZE	DESCRIPTION	BIT USED	MEM STATUS
0x1A00	4 bytes	not used		
0x1A04	4 bytes	Axial-pulse-area-Threshold1	10-0	R/W
0x1A08	4 bytes	Axial-pulse-area-Threshold2	10-0	R/W
0x1A0C	4 bytes	Axial-pulse-area-Threshold3	10-0	R/W
0x1A10	4 bytes	Axial-pulse-area-Threshold4	10-0	R/W
0x1A14	4 bytes	Axial-pulse-area-Threshold5	10-0	R/W
0x1A18	4 bytes	Axial-pulse-area-Threshold6	10-0	R/W
0x1A1C	4 bytes	Axial-pulse-area-Threshold7	10-0	R/W
0x1A20	4 bytes	not used		
0x1A24	4 bytes	z-and-stereo-pulse-area-Threshold1	10-0	R/W
0x1A28	4 bytes	z-and-stereo-pulse-area-Threshold2	10-0	R/W
0x1A2C	4 bytes	z-and-stereo-pulse-area-Threshold3	10-0	R/W
0x1A30	4 bytes	z-and-stereo-pulse-area-Threshold4	10-0	R/W
0x1A34	4 bytes	z-and-stereo-pulse-area-Threshold5	10-0	R/W
0x1A38	4 bytes	z-and-stereo-pulse-area-Threshold6	10-0	R/W
0x1A3C	4 bytes	z-and-stereo-pulse-area-Threshold7	10-0	R/W

- BAD-CHANNEL

The BAD-CHANNEL LUT stores the bad-channed-status bit for every and each strips. When a Strip is known to be bad its bad-channel-status bit must be set to '1'.

Note that the read out from this memory has bit 22 to 16 set as CHIP-ID and 3 bits of strip group (there are 8 groups of 16 strips per SVX chips).

BAD-CHANNEL					
PCI-Address[12-0]	SIZE	CHIP ID	Description	BIT USED	MEM STATUS
0x1800	4 bytes	0	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1804	4 bytes	0	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1808	4 bytes	0	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x180C	4 bytes	0	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1810	4 bytes	0	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1814	4 bytes	0	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1818	4 bytes	0	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x181C	4 bytes	0	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1820	4 bytes	1	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1824	4 bytes	1	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1828	4 bytes	1	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x182C	4 bytes	1	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1830	4 bytes	1	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1834	4 bytes	1	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1838	4 bytes	1	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x183C	4 bytes	1	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R

BAD-CHANNEL					
PCI-Address[12-0]	SIZE	CHIP ID	Description	BIT USED	MEM STATUS
0x1840	4 bytes	2	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1844	4 bytes	2	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1848	4 bytes	2	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x184C	4 bytes	2	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1850	4 bytes	2	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1854	4 bytes	2	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1858	4 bytes	2	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x185C	4 bytes	2	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1860	4 bytes	3	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1864	4 bytes	3	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1868	4 bytes	3	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x186C	4 bytes	3	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1870	4 bytes	3	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1874	4 bytes	3	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1878	4 bytes	3	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x187C	4 bytes	3	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R

BAD-CHANNEL					
PCI-Address[12-0]	SIZE	CHIP ID	Description	BIT USED	MEM STATUS
0x1880	4 bytes	4	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1884	4 bytes	4	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1888	4 bytes	4	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x188C	4 bytes	4	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1890	4 bytes	4	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1894	4 bytes	4	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1898	4 bytes	4	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x189C	4 bytes	4	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18A0	4 bytes	5	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18A4	4 bytes	5	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18A8	4 bytes	5	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18AC	4 bytes	5	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18B0	4 bytes	5	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18B4	4 bytes	5	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18B8	4 bytes	5	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18BC	4 bytes	5	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R

BAD-CHANNEL					
PCI-Address[12-0]	SIZE	CHIP ID	Description	BIT USED	MEM STATUS
0x18C0	4 bytes	6	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18C4	4 bytes	6	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18C8	4 bytes	6	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18CC	4 bytes	6	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18D0	4 bytes	6	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18D4	4 bytes	6	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18D8	4 bytes	6	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18DC	4 bytes	6	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18E0	4 bytes	7	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18E4	4 bytes	7	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18E8	4 bytes	7	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18EC	4 bytes	7	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18F0	4 bytes	7	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18F4	4 bytes	7	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18F8	4 bytes	7	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x18FC	4 bytes	7	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R

BAD-CHANNEL					
PCI-Address[12-0]	SIZE	CHIP ID	Description	BIT USED	MEM STATUS
0x1900	4 bytes	8	Strips 0 to 15 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1904	4 bytes	8	Strips 16 to 31 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1908	4 bytes	8	Strips 32 to 47 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x190C	4 bytes	8	Strips 48 to 63 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1910	4 bytes	8	Strips 64 to 79 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1914	4 bytes	8	Strips 80 to 95 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x1918	4 bytes	8	Strips 96 to 111 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R
0x191C	4 bytes	8	Strips 112 to 127 Chip(4-bit) and Group(3-bit)	15-0 22-16	R/W R

- TEST-LUT

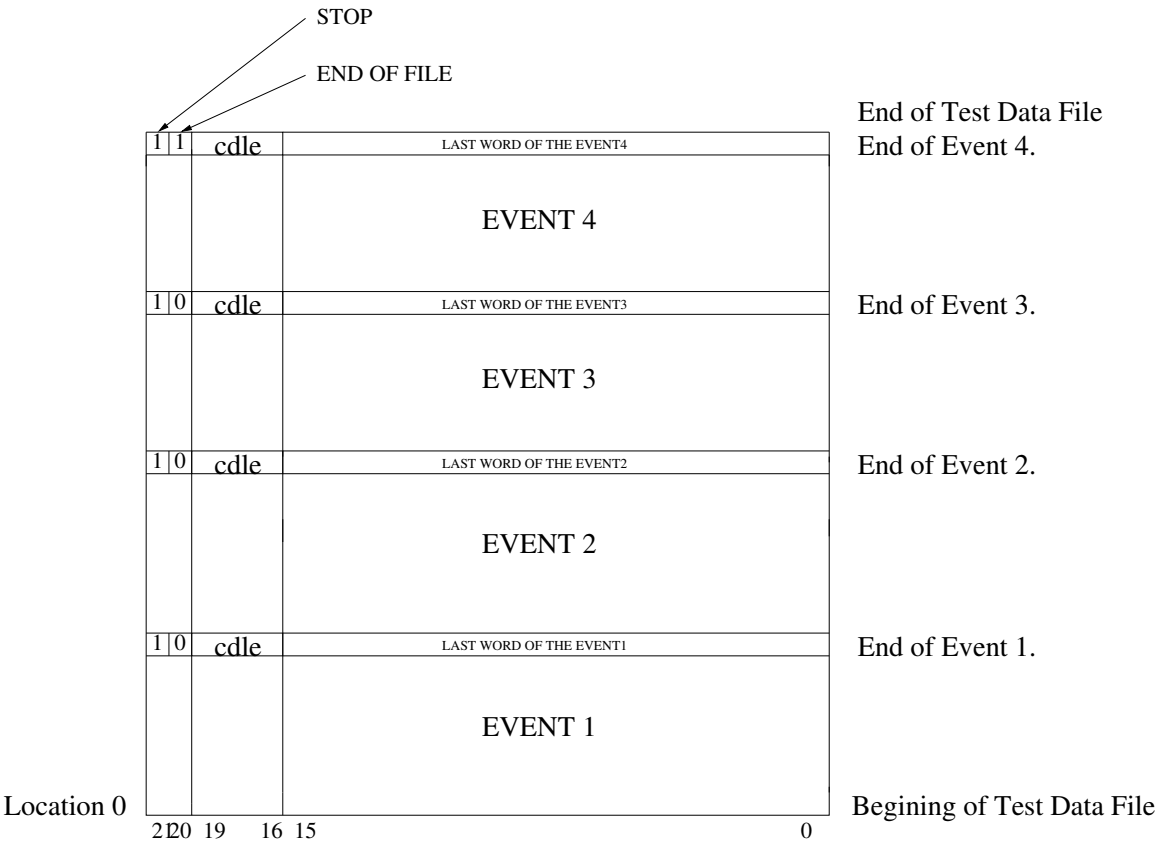
The TEST LUT stores the SMT TEST DATA for a pair of STC channels (i.e. 0 and 1, 2 and 3, 4 and 5, 6 and 7). Only one copy is stored which implies that bit 13 of the PCI3 address is ignored when accessing the TEST LUT.

PCI ADDRESS		
PCI-Address[12-0]	SIZE	MEM STATUS
0x1000	2032 bytes	R/W

DATA DESCRIPTION		
Description	bit used	
STOP set to 1 for end of event	21	
END OF FILE set to 1 for end of test file	20	
CAV for channel even and odd	19	
DAV for channel even and odd	18	
LNKRDY for channel even and odd	17	
ERROR for channel even and odd	16	
TEST DATA for channel odd	15-8	
TEST DATA for channel even	7-0	

Test Data file description:

The SMT-TEST-DATA file may include several events. The last word of an event must have the bit 21 set to 1 and the last word of the whole file must have both bits 21 and 20 set to one. An Example of Test data file is shown in the following chart:



NOTE: cdle = cav-dav-lnkrdy-error.

Figure 1: Test Data file example

This an example of how the TEST-SMT-DATA file looks like:

```
0x80505 =>  Event1 (Beginning of file)
0x80002
0x882c0
0x800c0
0x80ac0
0x803c0
0x80bc0
0x818c0
0x8c0c0
0x28c0c0 =>  End of Event1
0x80505 =>  Event2
0x80002
0x88280
0x80000
0x85152
0x8020e
0x85553
0x80c0a
0x856c0
0x805c0
0x8c0c0
0x38c0c0 =>  End of Event2 (End of file)
```

- GAIN-OFFSET

This Memory is used to correct SMT data for offset and scale. This is a Chip-To-Chip table and there are up to 9 chips mounted on a silicon detector.

PCI ADDRESS		
PCI-Address[12-0]	SIZE	MEM STATUS
0x0000	2304 bytes	R/W

The following address stores the corrected data for a given input ADC value for a given chip number:

Note that the VTM data value is used as byte address here. The byte contains the corresponding corrected data. The memory is READ/WRITE.

PCI Address Description	
Address	Description
PCI-Address$[12]_{hex}$	0x0
PCI-Address$[11\text{-}8]_{hex}$	CHIP-ID$_{hex}$ (from 0 to 8)
PCI-Address$[7\text{-}0]_{hex}$	$(Integer[\frac{VTM-DATA-VALUE_{dec}}{4}] \times 4)_{hex}$

NOTE: VTM-DATA-VALUE from 0 to 255.

DATA Description	
BIT USED	Description
31-0	4 Corrected data values(8-bits)

Each Corrected data is written into a given byte number from 0 to 3.
This is given by the following formula:

Byte number = Remainder$[\frac{VTM-DATA-VALUE_{dec}}{4}]$

1.2 CONTROL LOGIC

1.2.1 Road Memory:

The total road memory size is currently 8 Mbytes. It could be increased in case of more refined roads are needed. This memory is accessed with a 23-bit address:

- address(22): bank bit. Bank 1 is an exact copy of Bank 0. The copy does not need to be downloaded, it is done by the firmware.
- address(21 - 5): road address with individual bits specified as following:
  - address(21): S sign bit.
  - address(20 - 19): Pt bin.
  - address(18 - 16): Extended Pt information.
  - address(15 - 10): Relative ϕ
  - address(9 - 5): Relative sector address
- address(4 - 2): STC channel number.
- address(1 - 0): should always be 0 (always double word aligned).

To save VME memory space, road memory is accessed in pages of 64kbytes. A road memory page register ROAD-PA contains address bits 22 to 16. The 16 LSBs select within the page which is mapped to 0x00000 - 0x0FFFF

The data must take the following format:

- data(10 - 0): lower centroid number
- data(21 - 11): upper centroid number
- data(31 - 22): check bits for error detection and correction. They must be generated from data(21 - 0) using the following equations:

  data(22) <= not (data(0) xor data(1) xor data(3) xor data(4) xor data(6) xor data(8) xor data(10));

  data(23) <= data(0) xor data(2) xor data(3) xor data(5) xor data(6) xor data(9) xor data(10);

  data(24) <= not (data(1) xor data(2) xor data(3) xor data(7) xor data(8) xor data(9) xor data(10));

  data(25) <= data(4) xor data(5) xor data(6) xor data(7) xor data(8) xor data(9) xor data(10);

  data(26) <= data(0) xor data(1) xor data(2) xor data(4) xor data(5) xor data(7) xor data(10);

  data(27) <= not (data(11) xor data(12) xor data(14) xor data(15) xor data(17) xor data(19) xor data(21));

  data(28) <= data(11) xor data(13) xor data(14) xor data(16) xor data(17) xor data(20) xor data(21);

  data(29) <= not (data(12) xor data(13) xor data(14) xor data(18) xor data(19) xor data(20) xor data(21));

data(30) <= data(15) xor data(16) xor data(17) xor data(18) xor data(19) xor data(20) xor data(21);

data(31) <= data(11) xor data(12) xor data(13) xor data(15) xor data(16) xor data(18) xor data(21);

1.2.2 l3 memory

The total l3 memory size is 4 Mbytes and it is addressed with a 23-bit word. It is also accessed in pages of 64kbytes. An l3 memory page register L3-PA contains address bits 21 to 16. The 16 LSBs select within the page which is mapped to 0x10000 - 0x1FFFF. This space is only used for debugging purposes. For data taking, its contents are never directly accessed.

1.2.3 CONTROL-LOGIC registers:

- L3-DATA:

  This is a read-only area, assigned from 0x20000 to 0x27FFF. Data for each L3 event must be read starting at 0x20000 till the end. Skipping data words might cause loss of synchronization. Reading over the end of event is protected and will not cause errors. This space behaves like a prefetchable memory, although it is a fifo in essence. Moving the address back for more than 256 bytes might cause loss of synchronization. Once the last word of the event being read out, reading again at 0x20000 or 0x28024(l3 word count) will get the next event data or word count as the output.

- L3-PA: l3 memory page address register ⇒ 0x28000-0x28003 (R/W 32-bit)

- ROAD-PA: road memory page address register ⇒ 0x28004-0x28007 (R/W 32-bit)

- RUN-CTL: run control register ⇒ 0x28008-0x2800B
  This is a set/reset register.

  - write '0' has no effect
  - write '1' to bit n $<$ 16 sets bit n
  - write '1' to bit m $>$ 15 resets bit m-16

  - bit 0 run set during data taking
  - bit 1 test-mode set to use test data
  - bit 2 not used
  - bit 3 SCL-READY
  - bit 4 ZVC-ENABLE set to Output Z centroids to ZVC.
  - bit 5 Accept data with bad chip ID.
  - bit 6 Calculation bit set to use three strips to calculate centroid.
  - bit 7 Enable internal buffer control logic
  - bit 15-8 Channel enable (default disabled).
  - bit 19 SCL-DONE.
  - bit 31-24 Xilinx FPGA design version number.

- MISC-CSR miscelaneous control/status ⇒ 0x2800C-0x2800F.
  - Bits 15-0 are commands, they are pulsed and do not persist.
  - Bits 31-16 are registered.

  command write:

  - bit 0 reset all control and channel logic.
  - bit 1 reset road memory error flags.
  - bit 2 not used.
  - bit 3 reset hit event mismatch flags.
  - bit 4 MONITOR-START.
  - bit 5 test start.

  status read:

  - bit 0 L3 data available flag
  - bit 1 road memory correctable error.
  - bit 2 road memory non-correctable error.
  - bit 3 not used.
  - bit 4 MONITOR-DONE.
  - bit 5 pci2(altera) hit buffer full.
  - bit 6 pci2(altera) z centroid buffer full.
  - bit 7 level 3 buffer full
  - bit (15-8) Event mismatch flags for SMT channel 7-0.

- INIT-TIME: SCL init timer ⇒ 0x28010-0x28013 (R/W 32-bit).
  ⇒ bit(11 - 0).

- FRC-DL: Sets allowed timing skew between FRC data and SMT data 0x28014-0x28017 (R/W 32-bit).
  - Timing Skew ⇒ bit(7 - 0).
  - Module location information to be added to the l3 data header word ⇒ bit(15 - 8).

- L3-CONF: L3 data configuration word ⇒ 0x28018-0x2801B (R/W 32-bit).
  ⇒ bit(9-0) UNBIASED-L3
  ⇒ bit(25-16) NORMAL-L3

- SEC-OFFSET: Sector offset used in road address calculation ⇒ 0x2801C-0x2801F (R/W 32-bit).
  ⇒ bit(6 - 0) sector offset.
  NOTE: crate 1 must have offset value as 0x48 and all other crates must have offset value less than 0x40.

- TEST register ⇒ 0x28020 (R/W 32-bit).
  - bit 9 if set, get FRC test data from LRB.
  - bit 8 if set, use internal test clock instead of VTM strobe signals.
  - bit 7-0 used to set time skew between FRC test data and VTM test data.
    * if set to 0x80, skew is zero.
    * if set to 0xff, FRC data lag about 5 μs.
    * if set to 0x00, FRC data lead about 5 μs
- L3 Event word count register ⇒ 0x28024 (R/W 32-bit).
  This register contains the number of L3 data word for the current event. When the L3 data for that event have been read out, the register is updated.
- LRB monitor register ⇒ 0x28040 to 0x2807F (R/W 32-bit).
  This register stores sixteen 32-bit words of lrb-mon space information. The first ten words (0x40 to 0x64) store data from the LRB monitoring registers with the PCI configuration space from → 0x48 to 0x6C according to the LRB report on Eric Hazen's page:

  `http://ohm.bu.edu/~hazen/my_d0/TxRx/LRB_Report1_12.pdf`

FRC-TEST-DATA file:

The FRC-TEST LUT is not sitting in the STC Xilinx FPGA, it is located into the PCI1 inferface Altera Chip. This memory space can store up to 256, 32-bit words. It can be accessed through BAR1 of PCI1 ⇒ 0x000-0x3FF.

BAR0 of the PCI1 interface is used to save the LRB address. If its bit 2 is set to '1', The event number of FRC test data will start at 0 after reset and increment by 1 for each event sent, until it reaches 255 and then wrap around back to 0. This could be useful for testing event synchronization during a long test.

The first word of each event should be the total number of data words that it contains. The last word of the file should be 0x80000000. The following schematic shows the structure of the TEST-FRC-DATA file:

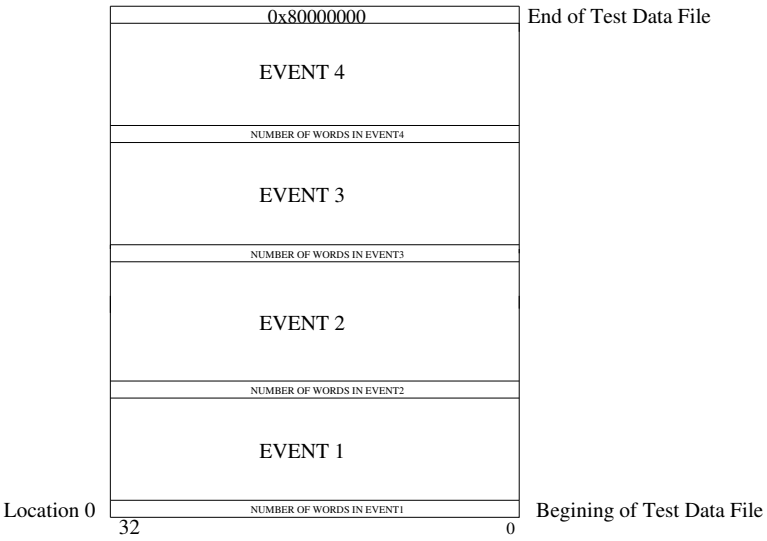


Figure 2: Test Data file example

Here is an example of a TEST-FRC-DATA file:

```
0xb =>  Number of word for Event1
0x23
0x1
0x4
0x5
0xcbd
0x6
0x7
0x8
0x9
0x23000000 =>  Event1 trailer
0xc =>  Number of word for Event2
0x24
0x2
0x4
0x5
0xabc
0x123
0x7
0x8
0x9
0xa
0x24000000 =>  Event2 trailer
0xd =>  Number of word for Event3
0x25
0x3
```

```
0x4
0x5
0xabc
0x234
0x345
0x7
0x8
0x9
0xa
0x25000000 =>  Event3 trailer
0x80000000 =>  End of file
```

Any comments on this document should be addressed to Alexandre Zabi: azabi@fnal.gov thanks!