# Specifications for the STC Control Logic

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August 22, 2002

## 1    Introduction

The STC control logic provides the interfacing between the three PCI-BUS interfaces and the eight sets of channel logic. Although the processing of SMT data into clusters and centroids, and the matching of FRC road data with the centroids to obtain hits occurs entirely within the eight sets of channel logic, control logic is needed to coordinate the operation of the channels. The principal functions performed by the control logic are:

- Respond to read or write commands of downloaded parameters from PCI-3.

- Return monitored data specific to the control logic to PCI-3.

- Retrieve L3 information from the channels for transmission to PCI-3.

- Read and save FRC data from PCI-1. The control logic formats this data into road information that is then sent to the channels.

- Transmit "hits" to the track fit card, TFC, and centroids to the Z vertex card, ZVC, (if the ZVC is implemented) via PCI-2.

## 2    FRC Data

32 bit FRC data, FRC-DATA, from PCI-1 is received in conjunction with three control signals, a write signal, FRC-WR, a header signal, HEADER, and a trailer signal, TRAILER. When HEADER is high, the T/R header word generated by the FRC is present using the format

| 31 ⋯ 20 | 19 ⋯ 16 | 15 ⋯ 8 | 7 ⋯ 0 | Bits |
|---------|---------|--------|-------|------|
|         | L1_QUAL |        | Event No. | Header |

When this header word is present on the data lines, the event number from the header is sent to the channel logic as FRC-EVENT simultaneous with a pulse on FRC-START. FRC-START is the AND of HEADER and FRC-WR. FRC-EVENT is used by the channel logic as the event ID to be added to the SMT data.

When TRAILER is high, a trailer word added by the FRC is present using the format

| 31 ⋯ 24 | 23 ⋯ 16 | 15 ⋯ 0 | Bits |
|---------|---------|--------|------|
| ERRORS  | Event No. |      | Trailer |

When neither TRAILER nor HEADER are high, the data is L1CTT information as received by the FRC. This data consists of a four word L1CTT header, followed by road data, followed by an L1CTT trailer.

Road data from the FRC must be stored in a FIFO for later readout, but a complication is that the header and trailer bits must also be stored, which means that the FIFO needs to be 34 bits wide. A 34 bit wide data path is undesirable because PCI-3 uses a 32 bit wide data path, hence, test data (to simulate FRC data) and L3 road data can only be 32 bits wide.

A solution to this dilemma is to use the MSB of the stored FRC data to indicate the presence of a header or trailer by moving the actual MSBs of the FRC data words to other unused bits, thereby allowing all FRC data to be stored as 32 bit words.

The modifications to the FRC data are:

- A T/R Header word is saved with the upper five bits as 11100 and shifting L1_QUAL down by eight bits so as not to lose the upper five bits.

- The MSBs of the four L1CTT header words are saved temporarily, allowing the MSBs of the stored header words to be cleared.

- The words following the four L1CTT Header words are assumed to be road words, which do not use bit 8, so their MSBs are moved to bit 8, so that all road words can be stored with their MSBs cleared. Bits 31 and 8 are also saved by being shifted through two four-bit shift registers. The outputs of these registers, X1 and X2, are the correct bits 31 and 8 of the L1CTT trailer.

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- Finally, the T/R trailer is saved as is but with its upper five bits as 11110 and replacing other unused bits with the previously saved MSBs and the X1 and X2 bits.

In the above procedure no provision is made for differentiating the L1CTT trailer from a road word, hence bits 31 and 8 of the L1CTT trailer have been altered. However, because bits 31 and 8 still exist as the X1 and X2 bits, the original L1CTT trailer can be reconstructed.

This procedure allows FRC road data to be saved in a 32 bit format format with minimal modification of the data.

In tabular form the stored FRC data appears as

| 31 | 30 ⋯ 27 | 26 ⋯ 24 | 23 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 ⋯ 9 | 8 | 7 ⋯ 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 11100 | | | | | | L1_QUAL | | | | | L1_BX | T/R Header |
| 0 | | | | | | | | | | | | | L1CTT Header-0 |
| 0 | | | | | | | | | | | | | L1CTT Header-1 |
| 0 | | | | | | | | | | | | | L1CTT Header-2 |
| 0 | | | | | | | | | | | | | L1CTT Header-3 |
| 0 | | | | | | | | | | | MSB | | Road |
| | | | | | ⋯ | | | | | | | | |
| 0 | | | | | | | | | | | MSB | | L1CTT Trailer |
| 0 | | | | | | | | | | | MSB | | Pad |
| 0 | | | | | | | | | | | MSB | | Pad |
| 0 | | | | | | | | | | | MSB | | Pad |
| | 11110 | | | X1 | X2 | MSB4 | MSB3 | MSB2 | MSB1 | ERRORS | | L1_BX | T/R Trailer |

L1_BX = Event Number
MSB1 = MSB of L1CTT Header-0
MSB2 = MSB of L1CTT Header-1
MSB3 = MSB of L1CTT Header-2
MSB4 = MSB of L1CTT Header-3
X1 = Bit 31 of L1CTT Trailer
X2 = Bit 8 of L1CTT Trailer

## 2.1 Test Data

For test purposes, an FRC test RAM is provided that can be loaded with test data. This data is loaded using the format shown above. The control logic reads data from this test RAM instead of from the normal FRC input FIFO when a bit called TEST has been set via PCI-3. The control logic monitors the TEST bit, and if it is set when new FRC data is about to be read, data from the test RAM is read rather than from the normal FIFO. An SMT-TEST bit is also output to the channels so that the channels also read input data from their SMT test FIFOs rather than from their usual input FIFOs. Only one block of FRC test data is allowed in the test RAM. Data

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is read from the test RAM starting from location zero and continuing until either the trailer bit is detected or the end of RAM is reached.

Note that there is no provision for sending FRC-EVENT to the channel logic when the test data is used, but this should not cause an event mismatch because the SMT should also be using test SMT data that has the same event number as the test FRC data. (When the channel logic is processing a test event, the event number that would be written to the trailer in the SMT FIFO is not being read anyway.)

It should also be noted that after processing a test event, a reset (equivalent to an SCL INIT) may be needed to resynchronize subsequent SMT and FRC data.

## 2.2   Processing of FRC FIFO Data

When all of the EVENT-BUSY signals from the channel logic are low, then no channel is processing event data and a block of data from the FRC input FIFO should be read. Words are read from the FIFO until a header word is found, indicated by the HEADER bit being set. From the header, the event ID (bits 0–7) is stored in a short EVENT FIFO for later use in generating the hit header word to the TFC. L1_QUAL from the FRC header is used to select one of two L3-CONFIG words. This word is output to the channel logic to indicate the types of L3 data that need to be generated and also to indicate whether or not this is a monitored event. A momentary signal EVENT-START is sent to the channel logic at the same time L3-CONFIG is output.

In response to EVENT-START, all channels set their EVENT-BUSY signals high. The control logic then reads an event number from the EVENT FIFO and outputs the hit header to PCI-2. Simultaneously, START-HITS is sent to the channels which pull their H-DONE signals low.

L1_QUAL has the following format in the T/R header. However, it is right-shifted by eight bits for internal storage and for L3 readout.

| 31 $\cdots$ 20 | 19 | 18 | 17 | 16 | Bits |
|---|---|---|---|---|---|
| | L1NoZeroSuppress | L2 UnbiasedSample | L2CollectStatus | L2ForcedWrite | |

If either bit 16 or bit 18 of L1_QUAL are high, then the configuration word UNBIASED-L3 is used to generate L3-CONFIG; otherwise NORMAL-L3 is used. The selected configuration word, plus the event, is also stored in a short FIFO used to control the readout of L3 data. This FIFO uses the following data format:

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| 20 | 19 · · · 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 · · · 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ROADS | CHANNEL | ROTATE | HITS | RAW | CORR | CLUSTER | AXIAL | STEREO | 90 | BAD | EVENT | |

Both UNBIASED-L3 and NORMAL-L3 have the following bit format:

| 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|
| ROADS | ROTATE | HITS | RAW | CORR | CLUSTER | AXIAL | STEREO | 90 | BAD | |

Each of the bits except for ROADS, ROTATE and BAD calls for a certain type of data to be output to a FIFO in the channel logic. BAD channel data already exists in a FIFO, so this FIFO does not need to be filled. AXIAL, STEREO and 90 refer to centroids, which are stored in a single FIFO, so a total of five L3 FIFOs are needed in the channel logic. ROADS also refers to an L3 FIFO, but this resides in the control logic rather than the channel logic. The meanings of the various bits are

- ROADS: Store all FRC data, including headers and trailers.

- ROTATE: This bit is used to limit the amount of data sent to level 3 by only allowing data from one channel to be stored in L3 FIFOs. This bit affects all data except HITS. A three bit counter in the control logic determines which channel is to be affected. Each event increments the counter, so with this bit set, eight events are needed to cycle through all channels.

- HITS: Store hits.

- RAW: Store raw data from the SMTs, data which have not been corrected for offset or gain or filtered by the bad channel mask.

- CORR: Store corrected data, data that have been corrected for offset and gain. Bad channels do not occur in these data.

- CLUSTER: Store clusters and associated strips.

- AXIAL, STEREO, 90: Store centroids for axial, stereo and 90 degree strips.

- BAD: Store the bad channel lookup table.

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The configuration word actually sent to the channel logic, L3-CONFIG, is derived from UNBIASED-L3 or NORMAL-L3 plus the L2CollectStatus bit from L1_QUAL. When the L2CollectStatus bit is set, a monitored event is specified, so the monitor bit in L3-CONFIG, MON is set. The format of L3-CONFIG is

| 12 | 11 ⋯ 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bits |
|-----|---------|--------|------|-----|------|---------|-------|--------|----|-----|------|
| MON | CHANNEL | ROTATE | HITS | RAW | CORR | CLUSTER | AXIAL | STEREO | 90 | BAD | |

where CHANNEL is the channel number specified by the three bit counter.

If the configuration word calls for L3 output of road data, then FRC data is written to the L3 FRC FIFO using a special format described later. A three bit FRC block counter is also incremented to indicate the number of blocks in the FRC FIFO.

The first four words of FRC data constitutes an L1CTT header. The first three of these are discarded, but the road counts for each of the four Bins are in the fourth header word and must be summed to obtain a total expected road count for the succeeding road data. The counts to be summed are in bits 0-5, 8-13, 16-21 and 24-29. This count is only used to determine the location of the L1CTT trailer.

Data words after the header contain road information. 17 bits from each of these are sent to the channel logic as ROAD-DATA, simultaneous with the ROAD-WRITE signal. Road words are read from the FRC input FIFO and sent to the channel logic until the expected road count is reached, a road count of 46 is reached or the T/R trailer is detected. If a road count of 46 is reached, additional words are read from the input FRC FIFO and discarded until the expected road count is reached. The word following the last expected road is assumed to be the L1CTT trailer and is discarded.

19 bits from each road word are used to generate the 17 bit road address for the channel logic. These are:

- S: The sign bit

- Ptbin: Two bits giving the Pt-Bin

- Ext Pt: Three bits of extended Pt information

- Relative phi: Six bits of relative address

- Trk Sector Address: Seven bits of sector address

A five bit offset is subtracted from the seven bit sector address to reduce the sector address to five bits. The format of the 17 bit road address sent to the channels is thus:

| 16 | 15 14 | 13 $\cdots$ 11 | 10 $\cdots$ 5 | 4 $\cdots$ 0 | Bits |
|---|---|---|---|---|---|
| S | Ptbin | Ext Pt | Relative phi | Trk Sector Addr minus Offset | |

The word following the L1CTT trailer should be the T/R trailer. The detection of this word stops the reading of further data from the FRC FIFO but the word itself is discarded, except for L3 readout. If the T/R trailer word is not detected, then a T/R trailer with bit 21 set (missing trailer, MT) is stored for L3 and readout of the FIFO is stopped.

Should the T/R trailer be detected before the expected number of words have been read from the FRC FIFO, then the L3 trailer is written (if L3 for roads is enabled by the configuration word) and the ROAD-END signal is sent to the channels.

The T/R trailer contains eight error bits from the link transmitter (bits 8–15) and a repeat of the event ID (bits 0–7). The error bits are included in the level 3 trailer and are also OR'd into bit RERR. RERR is later output in the hits trailer word.

After the T/R trailer is read, a ROAD-END signal is sent to the channel logic, allowing hit filtering to begin. Subsequent hit data comes automatically from the channel logic over HC-DATA in conjunction with HC-WR. HC-DATA goes directly to PCI-2, but the write signal to PCI-2, PCI-2-WR, is controlled so that the trailers from the various channels are rejected. Although each channel outputs a trailer at the end of its block of hit data, the control logic and not the channel logic should output the hit trailer to PCI-2. When signal H-DONE goes high, the control logic outputs this trailer. If Z-Vertex output is enabled, then the stereo header is output on the next clock cycle and a START-CENTROIDS signal is sent to the channels, causing the channels to pull their C-DONE signals low, after which stereo data is automatically output from the channel logic over HC-DATA. Similar to the hit data output, stereo data must also be buffered so that the trailers from individual channels can be rejected. When C-DONE goes high, the control logic outputs the stereo trailer word.

The data formats for hits sent to the TFC and centroids sent to the ZVC are

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### 2.2.1  Hits

| 31 ⋯ 28 | 27 | 26 | 25 | 24 | 23 | 22 ⋯ 16 | 15 ⋯ 13 | 12 ⋯ 9 | 8 | 7 ⋯ 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1100 | | | | | | | | | | EVENT | Header |
| TRACK | | | | dE/dx | | SEQ | HDI | CHIP | | STRIP | Hit |
| | | | | | ⋯ | | | | | | |
| 1111 | SERR | MM | RERR | EERR | | No. of Hits | | Link Error Bits | | EVENT | Trailer |

### 2.2.2  90 Degree Centroids

| 31 ⋯ 28 | 27 | 26 | 25 | 24 | 23 | 22 ⋯ 16 | 15 ⋯ 13 | 12 ⋯ 9 | 8 | 7 ⋯ 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1011 | | | | | | | | | | EVENT | Header |
| TRACK | | | | dE/dx | | SEQ | HDI | CHIP | | STRIP | Hit |
| | | | | | ⋯ | | | | | | |
| 1111 | SERR | MM | RERR | EERR | | No. of Centroids | | Link Error Bits | | EVENT | Trailer |

EVENT is the event ID from the FRC header and not the event added to the SMT data. SERR, MM, and EERR are the OR'd error bits from all of the channels. RERR is the OR of all of the link error bits from the FRC trailer.

These error bits, when set, indicate the following errors for each event:

- SERR: One or more SMT inputs had its ERROR bit set.

- MM: One or more SMT inputs had a mismatch between its received SEQ or HDI ID and its expected ID. This bit is also set if one or more SMT inputs did not have the msb set for its chip ID byte or if the byte after the chip ID was not zeros.

- RERR: One or more of the error bits in the FRC trailer word was set.

- EERR: One or more channels had a mismatch between its assigned event number and the event number from the FRC.

### 2.2.3  Generation of Road Address

The 17 bits of road address sent to the channels come from bits 0–6, 10–15 and 26–31 of each FRC road word. Bits 10–15 and 26–31 are used as is, but the sector address, bits 0–6, is reduced to five bits by subtracting a five bit crate offset, OFFSET, from bits 0–4 and ignoring bits five and six. The format of the 17 bit word is thus:

| 16 ⋯ 11 | 10 ⋯ 5 | 4 ⋯ 0 | Address to channels |
|---|---|---|---|
| 31 ⋯ 26 | 15 ⋯ 10 | (4 ⋯ 0) minus OFFSET | Bits from FRC road word |

### 2.2.4  L3 Format of Road Data

Road data for L3 is saved exactly as that data is saved in the FRC input FIFO, but with a missing trailer bit MT added to the trailer word. When set, MT indicates that the expected number of roads were read, but no T/R trailer word was present. Thus, the L3 format for FRC data is

| 31 | 30 ··· 27 | 26 ··· 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 ··· 9 | 8 | 7 ··· 0 | Bits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
|  | 11100 |  |  |  |  |  | | L1_QUAL | | | | | L1_BX | T/R Header |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | L1CTT Header-0 |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | L1CTT Header-1 |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | L1CTT Header-2 |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | L1CTT Header-3 |
| 0 |  |  |  |  |  |  |  |  |  |  |  | MSB |  | Road |
|  |  |  |  |  |  | ··· |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  | MSB |  | L1CTT Trailer |
| 0 |  |  |  |  |  |  |  |  |  |  |  | MSB |  | Pad |
| 0 |  |  |  |  |  |  |  |  |  |  |  | MSB |  | Pad |
| 0 |  |  |  |  |  |  |  |  |  |  |  | MSB |  | Pad |
|  | 11110 |  |  | MT | X1 | X2 | MSB4 | MSB3 | MSB2 | MSB1 | ERRORS | | L1_BX | T/R Trailer |

L1_BX = Event Number
MSB1 = MSB of L1CTT Header-0
MSB2 = MSB of L1CTT Header-1
MSB3 = MSB of L1CTT Header-2
MSB4 = MSB of L1CTT Header-3
X1 = Bit 31 of L1CTT Trailer
X2 = Bit 8 of L1CTT Trailer
MT = Missing Trailer

# 3  SCL INIT

If an SCL INIT is required, the following sequence occurs:

- Bit SCL_READY is set via PCI-3. When the control logic reads a high value for SCL_READY, it sends a CLEAR signal to all of the channels and initializes a 12 bit timer with a downloaded parameter INIT-TIME. At the 32 MHz clock frequency, this timer has a maximum delay of 128 $\mu$secs. While the wire-OR'd signal SMT-EMPTY from all of the channels is high, the timer is allowed to run. However, if SMT-EMPTY goes low, the counter is reinitialized and another CLEAR pulse is sent to the channels.

- When the timer "times out", the control logic sets bit SCL_DONE, indicating that all channels have remained free of input data for the

specified time interval and all FIFOs and logic have been reset (including the monitor registers). The control logic also clears and monitors its FRC input FIFO in conjunction with clearing and monitoring the channel logic so that setting of SCL_DONE also indicates that FRC data input has been idle for the specified time interval.

- After SCL_DONE has been set, SCL_READY will eventually be reset via PCI-3.

- When the control logic senses SCL_READY low, it resets SCL_DONE, completing the SCL INIT sequence.

# 4  Monitoring Handshaking

Two bits accessible via PCI-3, MON_DONE and MON_START, are used in the monitoring handshaking procedure. MON_DONE indicates when monitored data is available for readout via PCI-3. MON_START causes monitored data to be latched independent of the L1 qualifier.

If MON_START is set, the control logic sends MON to the eight channels and immediately sets MON_DONE. MON_DONE is cleared via PCI-3 after all monitored data have been read. When MON_START is not set, monitored data is latched in response to the appropriate L1 qualifier. In this case, MON_DONE is not set until all EVENT-BUSY signals from the channels are high and all hits and ZVC data have been output.

MON_DONE is also output to the FRC as wire-or'd signal PUT_DONE* via J3.

# 5  Monitoring Information

Four kinds of monitored data are generated by the control logic; the number of hits read from FRC data, the number of events, the number of hits sent to the TFC and the number of centroids sent to the ZVC. These are 24 bit values.

# 6 Readout of L3 Data

The readout of L3 data is entirely separate from the processing of an event. When all L3-DONE signals from the channels are high and the configuration FIFO is not empty, a word is read from this FIFO. The configuration part of the word is sent to all of the channels as START-L3. The event number from the FIFO is saved and also output in the header to the external L3 FIFO.

The bit format of START-L3 is

| 9 ⋯ 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bits |
|---|---|---|---|---|---|---|---|---|
| CHANNEL | ROTATE | HITS | RAW | CORR | CLUSTER | CENTROID | BAD | |

The output of L3 data on L3-DATA occurs automatically from the channel logic. The control logic writes this data to an L3 output FIFO for readout via PCI-3. This FIFO contains a header, written when START-L3 is issued, and a trailer, written when all L3-DONE signals go high. The format for data in this FIFO is:

| 31 ⋯ 27 | 26 | 25 ⋯ 8 | 7 ⋯ 0 | Bits |
|---|---|---|---|---|
| 10001 | | | EVENT | Header |
| | | | | L3 data |
| 11111 | T | | EVENT | Trailer |

The truncation (or T) bit in the trailer is set if the data in the FIFO was truncated. If the FIFO becomes full (the FIFO depth is 20,480 words) while event data is being written, all remaining L3 data from the present event are ignored ; as soon as the FIFO is no longer full, a trailer is written with the T bit set and acceptance of L3 data is re-enabled.

Readout of the FIFO via PCI-3 uses data lines L3-OUT rather than the Monitor/Download data lines DATA. This allows for faster readout of L3 data, since transfers via DATA are likely to use wait states.

# 7 Bus Enable

In order to prevent an overlap of signals on the hits/centroids data bus and the L3 data bus from two channels when one channel is connecting to a bus and the other is disconnecting, a quadrature clock signal, called BUS-ENABLE, is sent to the channels. The OR of this signal with the complement of the normal clock is used as a bus enabling signal in the channel logic. A 25% off interval is thus guaranteed between bus drivers of different channels, thereby ensuring that the buses will never be briefly driven by two channels during a transition between channels.

# 8 Interface Signals

The attached figure shows the interface signals for the control logic. These are:

- PUT_DONE*: A wire-or'd signal to J3 indicating that monitored data is available.

- CLEAR: A momentary signal sent to the channel logic to cause all FIFOs to be reset. It also causes other bits in the channel logic to be reset so that the channel logic is in an idle state.

- SMT-EMPTY: A wire-or'd signal from each channel indicating that all SMT input FIFOs are empty.

- FRC-START: A momentary signal sent to the channels when PCI-1 starts to output a new block of FRC data to the control logic.

- FRC-EVENT: An eight bit event number sent to the channels in conjunction with FRC-START. This number is derived from the FRC header word.

- MON: A momentary signal to the channels to cause immediate latching of monitored data.

- EVENT-START: A momentary signal to the channels indicating the start of event processing. This signal should cause one block of SMT input data to be read and processed.

- FRC-DATA: 32 bit FRC data received from PCI-1.

- FRC-WR: A write signal from PCI-1 for storing FRC-DATA in the FRC input FIFO.

- HEADER, TRAILER: Two bits from PCI-1 indicating the presence of a header or trailer in FRC-DATA.

- PCI-1-CLK: Clock provided by PCI-1.

- BUS-ENABLE: A delayed clock (1/4 cycle delay) used in conjunction with CLOCK to generate a bus-enabling signal for hits/centroids and L3 data to eliminate glitches due to two channels simultaneously driving the buses.

- HC-DATA: 32 bit hit or centroid data to PCI-2.

- PCI-2-WR: A write signal to PCI-2 when HC-DATA is valid.

- PCI-2-CLK: Clock to PCI-2.

- PCI-2-FF: A signal from PCI-2 indicating that the PCI-2 FIFO is full.

- ROAD-DATA: 17 bit road data to the channel logic. This data is used as the address to an external LUT associated with each channel.

- ROAD-WR: A write signal to the channels when ROAD-DATA is valid.

- ROAD-END: A momentary signal to the channels indicating that all road data for the current block of FRC data has been sent to the channels.

- CLOCK: The 32 MHz clock for the control logic.

- EVENT-BUSY: A signal from each channel indicating that the channel is busy processing an event and hence should not be signalled to begin processing a new event.

- HC-WR: A signal from each channel indicating valid HC-DATA.

- START-HITS: A momentary signal to the channels to cause them to start outputting one block of hits.

- START-CENTROIDS: A momentary signal to the channels to cause them to output one block of centroids.

- H-DONE: A signal from each channel indicating that all hits for the current event have been output over HC-DATA.

- C-DONE: A signal from each channe indicating that all centroid data for the current event has been output over HC-DATA.

- ZVC-ENABLE: A signal to the channels indicating that 90 centroids should be sent to the ZVC.

- L3-CLK: Clock to external L3 FIFO.
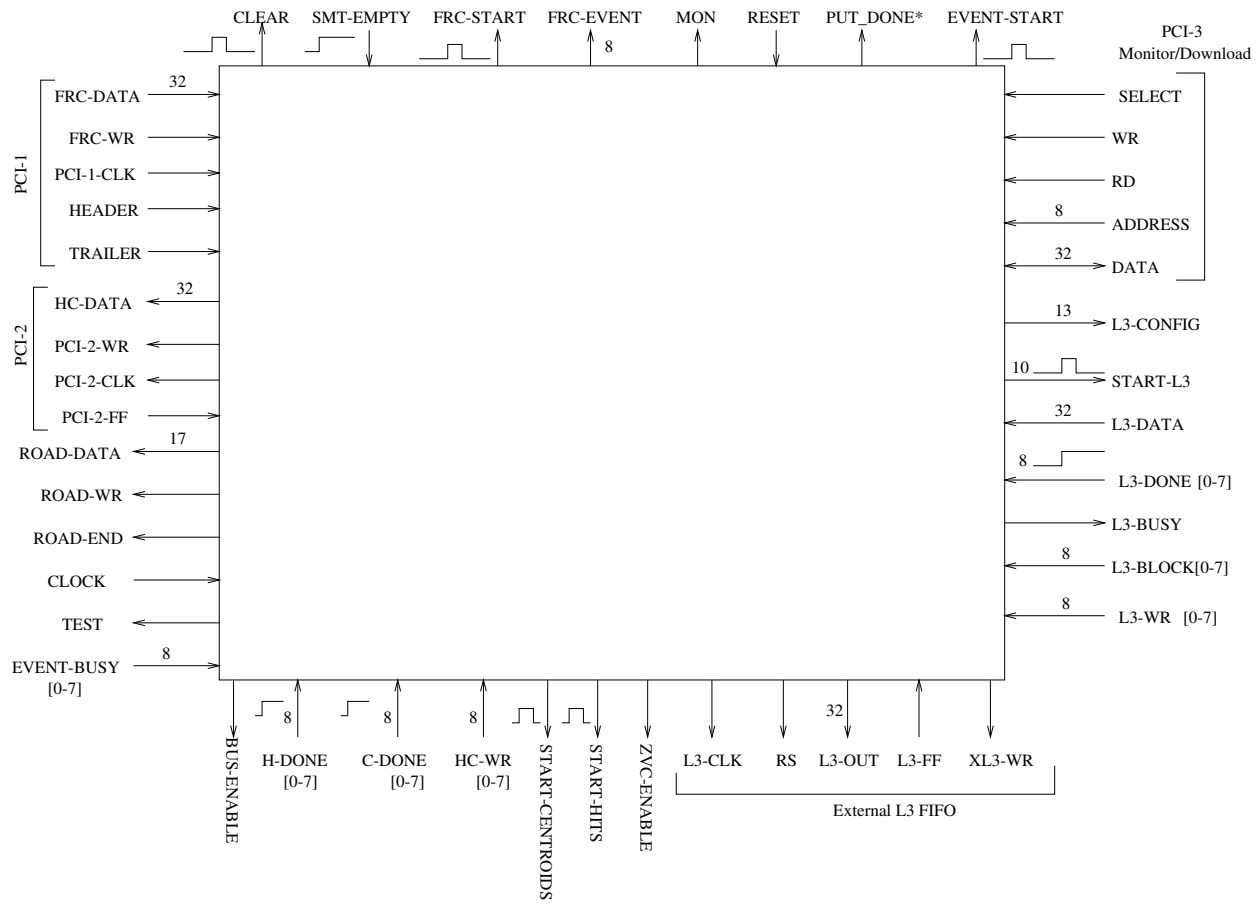
- RS: Reset to external FIFO.

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- L3-OUT: 32 bit L3 data to the external L3 FIFO.

- L3-FF: Full flag from the external L3 FIFO.

- XL3-WR: Write signal to the external L3 FIFO.

- SELECT: A signal from PCI-3 to enable reading or writing of PCI-3 data.

- WR, RD, ADDRESS, DATA: Control, address and data signals used in conjunction with the SELECT input of PCI-3.

- L3-CONFIG: A thirteen bit word to the channels, specifying the types of L3 data to be stored and whether or not this is a monitored event.

- START-L3: A ten bit word to the channels to initiate the readout of the L3 FIFOs.

- L3-DATA: 32 bit L3 data from the channels.

- L3-WR: A signal from each channel indicating that valid data exists on L3-DATA.

- L3-DONE: A signal from each channel indicating that L3 data blocks have been read for one event. The L3 FIFOs may still have data from other events, though.

- L3-BUSY: An inhibit signal sent to all of the channels to prevent them from outputting L3 data via L3-DATA. This is used when the control logic is outputting its L3 road data.

- L3-BLOCK[0-7]: Eight signals, one from each channel, indicating a channel that is in the process of outputting a block of L3 data. While any one of these signals is high, the control logic cannot start outputting its L3 data.

- RESET: Power-on reset signal.

# 9 Parameters Accessed by PCI-3

Several parameters must be downloaded to the control logic in order for it to function properly. Except for TEST-DATA, these can also be uploaded. SCL_DONE, MON_DONE and INIT-REQ are readable but not writeable via PCI-3.

- TEST-DATA: 32 bit FRC test data. This data is loaded into a test RAM for readout when the TEST bit is high.

- TEST: A bit that specifies using the downloaded test FRC data and test SMT data rather than data from the usual input FIFOs.

- NORMAL-L3: The normal 10-bit L3 configuration word used to specify the types of L3 data to be output.

- UNBIASED-L3: The 10-bit L3 configuration word used for unbiased samples.

- SCL_READY: A bit that causes initialization of the channel and control logic. Setting it does not, however, clear any previously downloaded parameters. This bit is set and reset externally via PCI-3.

- SCL_DONE: A bit set by the control logic after the SCL INIT procedure has been executed. This bit is reset by the control logic after SCL_READY goes low.

- MON_DONE: A bit set by the control logic when monitored data has been latched. It is cleared by the control logic when MON_READ goes high.

- MON_READ: A bit set by PCI-3 after monitored data has been read. It is cleared when MON_DONE returns low.

- MON_START: A bit set externally via PCI-3 to cause latching of monitored data. It is cleared when MON_DONE returns low.

- INIT-TIME: A 12-bit time delay used when INIT is set.

- ZVC Enable: A bit that enables output of 90 degree centroids to the Z vertex card.

- OFFSET: A five bit value used to reduce the seven bit sector address to five bits.

- SCL: A ten bit value holding the event mismatch bits for the eight channels plus HIT-ERR and the PCI-2 full bit.

CLEAR   SMT-EMPTY   FRC-START   FRC-EVENT   MON   RESET   PUT_DONE*   EVENT-START

PCI-3
Monitor/Download

FRC-DATA   32

FRC-WR

PCI-1-CLK

HEADER

TRAILER

PCI-1

SELECT

WR

RD

ADDRESS   8

DATA   32

HC-DATA   32

PCI-2-WR

PCI-2-CLK

PCI-2-FF

PCI-2

L3-CONFIG   13

START-L3   10

L3-DATA   32

L3-DONE [0-7]   8

ROAD-DATA   17

ROAD-WR

ROAD-END

CLOCK

TEST

EVENT-BUSY   8
[0-7]

L3-BUSY

L3-BLOCK[0-7]   8

L3-WR [0-7]   8

BUS-ENABLE   H-DONE   C-DONE   HC-WR   START-CENTROIDS   START-HITS   ZVC-ENABLE   L3-CLK   RS   L3-OUT   L3-FF   XL3-WR
                [0-7]    [0-7]    [0-7]
                  8        8        8                                                          32

External L3 FIFO

Interface Signals for the Control Logic