Specifications for One Channel of the STC Logic

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Abstract

This document provides functional and interface specifications for one channel of the STC logic. The complete STC daughtercard consists of eight of these channels plus some control logic to provide communication between these channels and the various PCI buses.

1 Introduction

The STC daughtercard contains eight identical blocks of channel logic, each designed to process data from one SMT input into clusters, centroids and hits (after road information is received from the FRC). External control logic manages the transfer of data between the channel logic and three PCI buses and also provides for overall control of the channel logic.

Silicon strip data arrives via an SMT input as a series of bytes following a prescribed data format. An input FIFO stores this data in double-byte format for later readout. When an EVENT-START signal is received from the control logic, data from the FIFO is read and processed into clusters and then centroids via special logic. These centroids are saved in a second FIFO for later readout by the hit filter, another block of special logic. The hit filter compares the centroids with road information provided by the Fiber Road Card, FRC, to determine "hits". After the external control logic has read the hit information, the channel logic reverts to waiting for another EVENT-START signal.

In addition to its primary function of determining "hits", the channel logic must create the level 3, L3, data and also the monitored data.

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The following sections provide detailed information on the operation of the channel logic.

2   SMT Data

SMT input data is received as a series of bytes in conjunction with a 53 MHz clock, STRBOUT, three control signals, CAV*, DAV*, LNKRDY* and an error signal, ERROR. Each data byte is valid when the corresponding DAV* and LNKRDY* signals are low and CAV* is high. When data is valid, the rising edge of the 53MHz clock, STRBOUT, stores a byte of SMT data plus the ERROR bit in a nine bit input register. Two input registers are needed to store a pair of SMT input bytes prior to the bytes being written to the SMT input FIFO.

The data format of the SMT byte sequence is:

```
Sequencer ID      0 to 255    (actual maximum is about 150)

HDI ID & Status   HDI ID uses bits 0-2, (HDI ID = 0 to 7)
                  Ignore the status bits.

Chip ID           0 to 8 (bits 0-3), MSB always 1

Hex 00

Channel ID        Strip number, 0 to 127, MSB always 0

Data              0 to 255
...               Channel ID and Data repeated for as many
...               as 127 strips. A new Chip ID followed
                  by 00 may also appear at any point.

Hex C0            Trailer C0
Hex C0            Trailer C0

Hex C0            Optional filler bytes
...
```

SMT input data are stored in the input FIFO as byte pairs (plus error bits), at an effective rate of 26.5 MHz, ensuring that the writing rate does not exceed the readout rate of 32 MHz.

A suggested data format for one block of SMT data in the 18 bit wide SMT FIFO is:

17	16	15 ⋯ 8	7 ⋯ 0	Bits
ERROR1	ERROR2	SEQ ID	HDI ID	
ERROR1	ERROR2	Chip ID	00	
ERROR1	ERROR2	Channel ID	Data value	
ERROR1	ERROR2	Channel ID	Data value	
		⋯		
ERROR1	ERROR2	Channel ID	Data Value	
ERROR1	ERROR2	C0	Event	Trailer

ERROR1 is associated with the more significant byte and ERROR2 with the less significant byte.

All data from the SMT is stored exactly as received (plus error bits), except for the trailer. The trailer replaces the second C0 with an event number, the source of which is descibed in the next section.

Note that additional C0 filler bytes following the initial C0C0 input trailer are not written to the FIFO. Only when a non-C0 SMT byte occurs does FIFO data storage resume.

2.1 Adding an Event Number to the SMT Trailer

SMT data does not arrive with any event identification, but to detect an event mismatch between FRC and SMT data blocks, event identication needs to be added to each SMT data block; this is done by writing an event number in the SMT trailer word.

In normal operation, the receipt of FRC data containing the event number occurs very close in time to the receipt of the SMT data for the same event, but it cannot be guaranteed that the event number from the FRC data will be received before the trailer of SMT data needs to be written. To ensure that the SMT trailer has the associated FRC event number, a time delay from the start of non-C0 SMT data and the writing of the trailer to the SMT FIFO is needed. This delay is generated by an 8-bit down-counter that is preset with a downloadable time delay when SMT data is recognized. Writing of the SMT trailer waits until the delay has expired and then is written with an event number FRC-EVENT that has been latched by FRC-START. At a 32 MHz clock rate, the maximum delay is about 8 μsecs.

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Obviously, if FRC-START occurs before the SMT data begins, no delay is needed. Also, as soon as FRC-START occurs, the delay can be terminated. These two conditions can be accomodated, with a resultant improvement in performance, by altering the way the delay counter operates, as follows: Both FRC-START and the start of SMT data are allowed to start and reset the counter; whichever signal occurs first starts the counter, the other signal resetting it. If both signals occur simultaneously, the counter is not started. When the SMT trailer is detected, writing of the trailer to the FIFO waits until the counter is idle (holds a count of zero).

It is not possible to confuse a C0 filler byte with a legal Sequencer ID, indicating the start of a new block of data, because the Sequencer ID has an actual maximum value of about 150 (96 hex).

2.2   Initiating Readout of the SMT FIFO

Data stored in the SMT FIFO is not read until the start of an event has been recognized. This start-of-event signal EVENT-START is sent by the control logic that reads the FRC road data. Besides initiating the clustering algorithm, EVENT-START latches a nine bit word, L3-CONFIG, eight bits specifying which of the eight types of L3 data must be stored during event processing, and one bit specifying whether or not this is a monitored event. EVENT-START also causes EVENT-BUSY to go high, signalling the control logic that an event is currently being processed.

In addition to the SMT FIFO, there is a second FIFO that is read instead of the SMT FIFO if input signal TEST is high. This second FIFO allows the channel logic to be tested using simulated SMT data.

2.3   Interpreting SMT Input Data

The first word read from the SMT FIFO, minus the ERROR bits, is saved as the SEQ ID and the HDI ID. These IDs are compared with expected values (downloaded parameters), a comparison mismatch setting an error bit MM and incrementing an associated error counter used for monitoring.

The next SMT word contains the chip number and a byte of zeros, but if the MSB of the word is not set, or if there is not a byte of zeros, MM is set and the associated counter incremented. The chip number, a value from 0 to 8, is compared with downloaded chip ranges for each data type to determine if the data is axial, stereo or 90 degree. All three data types are processed

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into clusters and centroids, but only axial centroids are passed to the hit filter logic.

The remaining SMT words are read as byte pairs, the upper byte being the strip number (called the channel ID in the SMT data) and the lower byte the data value from the strip. The first byte of these pairs always has an MSB of 0. If The MSB is 1, then this indicates a new chip number and the second byte of the pair should be zero as with the initial chip number.

If either error bit from any FIFO word is set, then an error bit SERR is set.

As SMT strip data are read from the input FIFO, some preprocessing is performed before the data are passed to the clustering function.

When a particular strip in a detector is known to be bad, its data value must be ignored (zeroed). To do this, a 1152×1 lookup table addressed by the four-bit chip number and the seven-bit strip number is examined to determine the good/bad status for each strip.

The value of each good strip must be corrected for offset and scale by consulting a second lookup table. This is a 2304×8 table addressed by the four-bit chip number and the eight bit data value.

Both of these tables for each of the SMT inputs must be initialized prior to use of the STC card.

2.4 Cluster Finder

After the strip data have been input and preprocessed (bad channels rejected, data corrected), a clustering algorithm is invoked. The baseline algorithm treats every contiguous group of channels above a (first) threshold as a cluster. Dead channels are treated as having zero pulse height. The channel with the highest pulse height in the cluster is the cluster center. Only channels having data values above a (second) threshold are allowed to be cluster centers. There are separate thresholds for axial, stereo and 90-degree channels; these are downloaded parameters.

In addition to identifying clusters, the Cluster Finder calculates a pulse-height weighted effective cluster center, called a centroid, centered on the cluster center. The nine most significant bits of this centroid replace the seven bits of the original cluster center, the effect being that of a four-fold improvement in resolution of the cluster center.

A pulse area (dE/dx) of the cluster is calculated by summing the data values for these n strips of each cluster and comparing them to three down-

loaded threshold values. Two bits are set to indicate the cluster pulse area according to the following scheme:

bits	dE/dx
00	$< T_1$
01	$\geq T_1, < T_2$
10	$\geq T_2, < T_3$
11	$\geq T_3$

For each cluster, the centroid information consists of two dE/dx bits, the four-bit chip ID and the calculated nine-bit centroid address.

Axial centroids are stored in a FIFO for subsequent readout to the hit filter. 90 degree centroids are stored in a separate FIFO for readout to the Z Vertex Card, but only if Z Vertex readout is enabled. If centroid readout to L3 is specified by the L3 configuration word, then all centroids are also stored in an L3 FIFO.

2.5 Hit Filtering

Hit filtering compares centroids from the cluster finder with road information from the FRC to determine hits. The road information is sent to a 128k×22 road LUT as a series of 17 bit values, the number of values lying between 0 and 46. From this LUT the channel logic obtains 11 bit lower and upper range limits for centroids, four bits specifying the chip number and seven bits specifying the strip. These range limits are stored in consecutively numbered register pairs for later comparison with centroids.

After the last road value has been received and translated into range limits, the centroids stored in the axial centroid FIFO are compared one at a time with all of the range limits. Any centroid falling within one of the ranges results in storing a corresponding "hit" bit (up to 46 of these) plus dE/dx, SEQ, HDI, the chip number and nine bit strip number in a 72 bit wide hit FIFO. SEQ in the FIFO words is reduced to a seven bit value by omitting bit 3 from the original eight bits of SEQ. After the last centroid has been used in hit generation, a trailer is written to the hit FIFO, this trailer containing the event number read from the FRC header. The trailer is identified by its 46 "hit" bits being zero.

The event number from the centroid data (the event assigned to the SMT data) is compared with the FRC event number when the centroid trailer is

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read. If these event numbers are not the same, an event error bit EERR is set. This bit is sent to the control logic and is only cleared after H-DONE goes high.

The same data written to the hit FIFO is also written to an L3 FIFO; this is not the L3 FIFO used for output of hit data to L3 but rather an interim FIFO from which the hit data is expanded. The 72 bit wide hit data in this FIFO is automatically expanded into individual 32 bit wide hits in the L3 hit FIFO. As opposed to the random readout of hits from different channels to the TFC, the expansion of hits for L3 readout must be done on a per-channel basis.

3 Hit and ZVC Data

Hit data for output to the TFC and 90 degree centroid data for output to the Z Vertex Card (ZVC) are stored in FIFOs and then output to the control logic. Data is only written to the 90 degree FIFO if the input signal ZVC-ENABLE is high. Data in these FIFOs is always terminated by a trailer word after all data for the current event has been processed. There is no header word, but the trailer must always be written for each event, even if there was no preceding data.

The event number in the trailer is the event number from the header word of the FRC data.

Data from the hit FIFO needs to be expanded into individual hits as it is output to the control logic, since each word in the hit FIFO may contain up to 46 hits.

The data formats for hits and centroids sent to the control logic are:

3.0.1 Hits

31 ⋯ 27	26	25 24	23	22 ⋯ 16	15 ⋯ 13	12 ⋯ 9	8	7	6	5	4	3 ⋯ 0	Bits
TRACK		dE/dx		SEQ	HDI	CHIP				STRIP			Hit
					⋯								
11110				EVENT		No. of Hits		SERR	MM	RERR	EERR		Trailer

3.0.2 ZVC Centroids

31	30 29	28 27	26	25 24	23	22 ⋯ 16	15 ⋯ 13	12 ⋯ 9	8	7	6	5	4	3 ⋯ 0	Bits
0	TYPE	SMT		dE/dx		SEQ	HDI	CHIP				STRIP			Centroid
						⋯									
11110				EVENT			No. of Centroids			SERR	MM	RERR	EERR		Trailer

3.1 The Data Transfer Process

The output of hit data over the HC-DATA lines occurs in response to momentary signal START-HITS from the control logic. The channel then pulls its H-DONE signal low and outputs its hits data via HC-DATA, provided that channel is not inhibited by an HC-BUSY signal from another channel. Data to HC-DATA is enabled only when BUS-ENABLE is high, thereby preventing glitches at the transition between channel switching. H-DONE remains low until all hits for that channel have been output to the control logic.

When all H-DONE signals are high, and if Z-ENABLE is high, the control logic outputs START-CENTROIDS to the channels, causing the channels to set their C-DONE signals low and to output centroids. C-DONE remains low until all centroids for that channel have been output.

By connecting the HC-BUSY signal from each channel to the HC-INH inputs of the higher numbered channels, hit and centroid transfer from all channels occurs without the need of any further signals from the control logic.

4 Monitoring Information

Monitoring information is latched when the L1 qualifier word from the FRC specifies a monitoring event and the channel logic has finished processing the event. The actual latching of monitored information occurs when EVENT-BUSY goes low. A bit in L3-CONFIG specifies whether or not this is a monitored event.

A signal MON from the control logic also causes the latching of monitored information, but this signal causes immediate latching and does not depend on the end of event processing.

All of the monitored data consists of registers (usually counters). These keep track of SMT errors, the number of centroids, etc. When the counters are latched, the counters themselves are cleared but continue operating, so a latched readout register is needed for each counter.

All of the monitoring registers should be accessible as consecutive memory locations so that the readout of monitoring can be done in burst mode rather than as a series of individual data transfers.

The monitored data are:

- A 24 bit SMT error count, the total number of times ERROR is high

during input of SMT data.

- A 24 bit SMT mismatch count indicating the number of times SMT data was received with an incorrect header, a mismatched Sequencer ID and/or HDI ID.

- Nine 24 bit "chip" counters, one for each possible SVX readout chip. Each of these is incremented whenever a strip data word is output from that particular chip.

- The total number of axial centroids , 24 bits.

- The total number of stereo centroids, 24 bits.

- The total number of 90-degree centroids, 24 bits

5   Level 3 (L3) Data

Although the primary function of the channel logic is the generation of hit information, it must also provide for saving the intermediate information used in the hit-generating process as L3 data. This intermediate information consists of raw SMT data, corrected SMT data, clusters, centroids, etc. Each of these data types is stored in a FIFO for later readout by the control logic. When an EVENT-START is received by the channel logic, a thirteen bit L3 configuration word, L3-CONFIG, is latched. This configuration word tells the channel logic which types of L3 data must be stored in FIFOs as the logic performs its normal event processing.

L3-CONFIG has the following format:

12	11 ⋯ 9	8	7	6	5	4	3	2	1	0	Bits
MON	CHANNEL	ROTATE	HITS	RAW	CORR	CLUSTER	AXIAL	STEREO	90	BAD	

where the meanings of the various bits are:

- MON: Indicates that this is a monitored event, meaning that monitored values must be latched at the end of event processing.

- CHANNEL: The channel number to be used in conjunction with RO-TATE.

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- ROTATE: A bit used to limit the amount of data to be sent to Level 3 by only allowing data from one channel to be stored in L3 FIFOs. This bit affects all data except HITS. When this bit is set, CHANNEL specifies the channel that is supposed to store L3 data.

- HITS: Store hits.

- RAW: Store raw data from the SMTs, data which have not been corrected for offset or gain or filtered by the bad channel mask.

- CORR: Store corrected data, data that have been corrected for offset and gain. Bad channels do not occur in these data.

- CLUSTER: Store clusters and associated strips.

- AXIAL, STEREO, 90: Store centroids for axial, stereo and 90 degree strips.

- BAD: Store the bad channel lookup table.

5.1 L3 Data Formats

This section gives data formats for the L3 buffers, each buffer being a 32 bit wide FIFO.

Each buffer may contain multiple data blocks (from more than one event), each block beginning with a header word and ending with a trailer word. These words exist even if there is no intervening data in the buffer. The most significant five bits of the header word identifiy the type of data in the buffer, raw data, corrected data, etc. Some header words may contain additional information such as the Sequencer ID and HDI ID. The most significant five bits of each trailer word are always 11110. The trailer also contains an event number, the event number from the trailer word of the SMT FIFO. The MSB of any intervening word, a data word, is always a zero, except in the HITS buffer. In the HITS buffer, TRACK numbers greater than 31 will result in the MSB (bit 31) being set, but this will not prevent the trailer from being recognized, since the trailer will have its upper four bits set.

Associated with each L3 FIFO is a three-bit block counter, indicating the number of complete blocks of L3 data in the FIFO. The L3 readout logic uses these block counters to ensure that it only outputs complete L3 blocks rather than get delayed waiting for a FIFO to fill.

5.2 Raw Data

31	30···27	26	25 24	23	22···18	17	16	15···13	12···8	7	6···0	Bits
	10000		SMT		SEQ			HDI	EVENT			Header
0						ERROR1	ERROR2	1ST BYTE		2ND BYTE		Data
						···						
	11110				EVENT					SERR		Trailer

SERR is the error bit set when the ERROR signal from the SMT is high. SERR in the trailer indicates that SERR was set in at least one of the data bytes. This bit is also included with data as it passes through the normal data processing algorithms.

SEQ and HDI are the expected (or downloaded) parameters and not the values from the SMT data stream.

5.3 Corrected Data

31	30 29	28 27	26	25 24	23	22···16	15···13	12···9	8	7	6	5···2	1 0	Bits
	10010			SMT		SEQ	HDI			EVENT				Header
0	TYPE					VALUE		CHIP		STRIP			00	Data
						···								
	11110					EVENT			SERR	MM				Trailer

MM is a bit that is set when the Sequencer ID and HDI ID don't match the expected values (downloaded parameters). It is also set if the first chip number byte does not have its MSB set or if the byte after any chip number is not zero. SEQ and HDI in the header and trailer words are the parameters read from the SMT; they are not the downloaded parameters. SMT specifies one of the eight SMT's. TYPE identifies the type of SMT data, axial, stereo or 90 degree.

The format for TYPE is:

22	21	Data Type
0	1	Stereo Strip
1	0	Axial Strip
1	1	90 Degree Strip
0	0	Undefined

5.4 Clusters/Strips

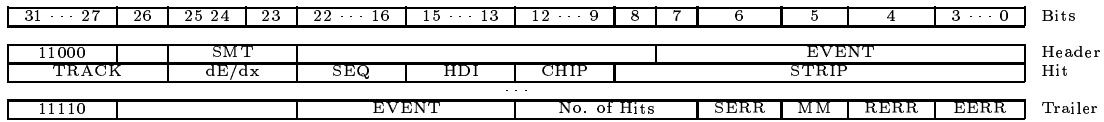| 31	30 29	28	27	26	25 24	23	22···20	19···16	15···13	12	11···9	8	7	6	5···2	1	0	Bits
	10100				SMT		SEQ	HDI					EVENT					Header
0	TYPE	3/5			THRESHOLD 1			THRESHOLD 2			STRIP COUNT						1	Cluster
0	TYPE						VALUE			CHIP			STRIP			0	0	Strip
							···											
	11110						EVENT					S	M					Trailer

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S=SERR and M=MM.

Following each cluster are the strips from which the centroid of the cluster was calculated. The strip having the largest data value is the center of the cluster, about which the centroid will be calculated. THRESHOLD 1 is the threshold that a strip value must equal or exceed in order to be included in a cluster. STRIP COUNT is the number of strips in the cluster with values equal to or greater than THRESHOLD 1. THRESHOLD 2 is the threshold that a strip value must equal or exceed in order to be a cluster center.

Bit 28, the 3/5 bit, indicates whether 3 or 5 strips will be used in the centroid calculation, a 0 indicating 3 strips and a 1 indicating 5 strips.
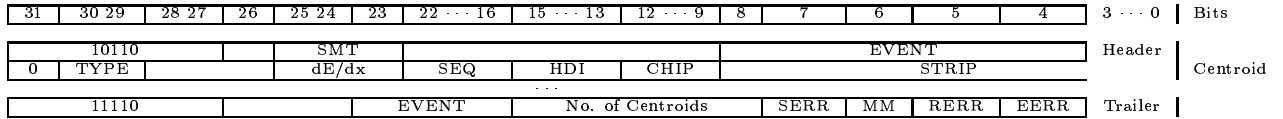
Bit 0 is used to differentiate strip words from cluster words.

5.5 Hits

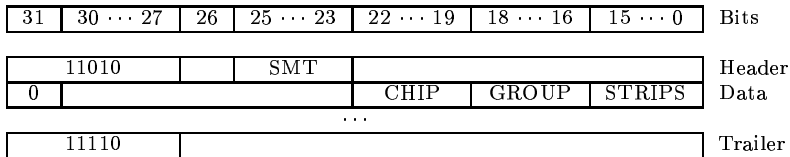| 31 ··· 27	26	25 24	23	22 ··· 16	15 ··· 13	12 ··· 9	8	7	6	5	4	3 ··· 0	Bits
11000		SMT							EVENT				Header
TRACK		dE/dx		SEQ	HDI	CHIP			STRIP				Hit
					···								
11110				EVENT		No. of Hits			SERR	MM	RERR	EERR	Trailer

TRACK is the track number from the FRC; it has a possible range of 1 to 46. RERR is set when an error occurred when reading road data from the FRC.

5.6 Centroids

31	30 29	28 27	26	25 24	23	22 ··· 16	15 ··· 13	12 ··· 9	8	7	6	5	4	3 ··· 0	Bits
	10110			SMT							EVENT				Header
0	TYPE			dE/dx		SEQ	HDI	CHIP			STRIP				Centroid
							···								
	11110					EVENT		No. of Centroids			SERR	MM	RERR	EERR	Trailer

5.7 Bad Strips

Bad strip data for L3 readout is not actually written to an L3 FIFO for each event. Rather a special memory holding bad strip data is written when data for the bad strip LUT is downloaded. This memory is read whenever bad strip L3 data is needed. SEQ, HDI and EVENT are not included in the header or trailer words.

31	30 ··· 27	26	25 ··· 23	22 ··· 19	18 ··· 16	15 ··· 0	Bits
	11010		SMT				Header
0				CHIP	GROUP	STRIPS	Data
			···				
	11110						Trailer

STRIPS contains the good/bad bits for 16 of the possible 128 strips, and hence, there need to be eight of these for all 128 strips of each chip. GROUP identifies the particular group of 16 strips. For the nine possible chips, 72 data words are needed for the complete BAD STRIP readout. A "one" bit indicates a bad strip.

5.8   Readout of L3 Data

Readout of L3 data is initiated by START-L3, a ten bit word from the control logic specifying which L3 FIFOs are to be read. At least one bit of this word is high. All channels now pull L3-DONE low and the lowest-numbered channel having a block of data for output generates an L3-BUSY signal to the higher-numbered channels as an inhibit input and also sets its L3-BLOCK signal high to retain control of the output bus, L3-DATA, until the complete data block has been output. At the completion of the block transfer, L3-BLOCK and L3-BUSY go low, allowing another (or the same) channel or the control logic to output a block of data. When all blocks for a given channel have been output, that channel sets its L3-DONE high as a signal to the control logic that all blocks for that channel have been output.

As with hit and centroid output, the L3-DATA lines should only be driven when signal BUS-ENABLE is high.

Signal L3-WR, is pulled high when data is present on L3-DATA.

Since there may be several blocks of data in each channel, a priority scheme must be implemented within each channel to control the selection of the blocks.

6   Interface Signals

The attached figure shows the interface signals required for each set of channel logic.

The SMT signals need little discussion. SMT data and the ERROR bit are stored in an SMT input FIFO when DAV* and LNKRDY* are both low until two consecutive C0 characters are received. Data storage is only resumed when a non-C0 character is received. SMT ID is a three bit identification code that is hard-wired on the daughtercard.

The remaining interface signals are:

- CLEAR: A momentary input that causes all FIFOs to be reset. It also resets other bits needed to put the channel logic in an idle state.

- SMT-EMPTY: A logic level indicating an empty SMT input FIFO.

- FRC-START: A momentary signal that occurs when a new block of FRC data begins arriving from the FRC.

- FRC-EVENT: An eight bit event number associated with new FRC data. This is latched by FRC-START

- EVENT-START: A momentary signal (one clock period) indicating that FRC data for an event is about to be sent to the channel logic. This should set an EVENT-BUSY bit which in turn should cause the reading of one block of SMT data as well as its clustering.

- MON: A momentary signal that causes monitored data to be latched immediately. Latching does not wait for the completion of event processing.

- ROAD-DATA: This is 14 bit road data from the FRC that is used as the address for the road LUT. It is also used to receive an event number in conjunction with EVENT-START.

- ROAD-WR: A momentary signal used to latch the 22 bits of data from the road LUT.

- RD-LUT: Read signal to the road LUT.

- WR-LUT: Write signal to the road LUT.

- ROAD-END: A momentary signal present with Road Write to indicate the last road from the FRC. This signal initiates the hit filtering operation by setting a Hits-Busy bit and it also resets the road (or track) counter used when storing road data.

- EVENT-BUSY: A signal indicating that the channel logic is processing data for an event. This signal goes high immediately after EVENT-START goes high and only goes low after the event has been processed, all hits have been determined and stored in the hit FIFO, all 90 degree centroids have been stored in the centroid FIFO and all L3 data

except hits have been generated and stored in their respective FIFOs. If monitoring was requested for the event, then the monitored data is latched immediately after the fall of EVENT-BUSY.

- HC-DATA: 32 data lines that output hits or centroids.

- HC-WR: A signal indicating that valid data exists on HC-DATA.

- H-DONE: H-DONE goes high when the last hit for one event has been output from the hit FIFO.

- ALL-H-DONE: A signal from the control logic indicating that H-DONE is high for all channels .

- C-DONE: C-DONE goes high when the last 90 degree centroid has been output from its FIFO.

- HC-BUSY: This is an inhibit signal that is sent to all of the higher numbered channels to inhibit those channels from outputting data.

- HC-INH: These are the seven inhibit inputs that receive inhibit signals from the lower channels. Channels 0 through 6 have fewer than seven inhibit signals from lower channels, so these unused inputs are wired low on the STC motherboard.

- L3-CONFIG: Thirteen bits indicating L3 data to be stored, plus one bit indicating a monitored event. These bits are latched by the EVENT-START signal.

- START-L3: A ten bit momentary word from the control logic to initiate readout of the L3 FIFOs. Each bit corresponds to one of the L3 FIFOs.

- L3-DATA: 32 data lines carrying the output data from the L3 FIFOs.

- L3-WR: A signal indicating that valid data exists on L3-DATA.

- L3-DONE: A signal indicating L3 data blocks have been read from all of the FIFOs for one event. This does not, however, mean that the FIFOs are empty.

- L3-BUSY: An inhibit signal sent to all higher channels to inhibit those channels from outputting data. Similar to HC-BUSY.

- L3-INH[0-7]: Similar to HC-INH[0-6], but with an eighth bit from the control logic.

- L3-BLOCK: A signal to all other channels and to the control logic indicating that this channel is outputting a block of data and that no other channel or the control logic is allowed to output data until the block has been completely transferred.

- L3-BLOCK-IN: The seven L3-BLOCK signals from the other channels.

- SELECT: A single bit input used to select the logic for writing or reading monitor and downloaded data.

- WR, RD, ADDRESS, DATA: Control, address and data signals used in conjunction with the SELECT input.

- ZVC-ENABLE: A level input from the control logic that enables the filling of the 90 degree centroid FIFO with data for the ZVC.

- TEST: An input signal that causes the test FIFO to be read rather than the SMT input FIFO when a new event is processed.

- BUS-ENABLE: A 75 % duty cycle signal for enabling signals onto the L3 readout bus and the hits/centroids. This signal eliminates glitches by preventing the overlapping of bus signals from different channels.

- RESET: A power-on reset signal.

7 Downloaded Parameters

The channel logic requires a considerable amount of downloaded information; this consists of lookup tables (LUTs), parameter values and individual bits, all sent to the channel logic via PCI-3.

The downloaded information is:

- Bad Strip LUT: This is an 1152×1 table. It may be downloaded as 36 32-bit words.

- Gain/Offset LUT: A 2304×8 array. When addressed with a four bit chip number and an eight bit data value, it provides a corrected eight bit output.

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- Road LUT: A 128k×22 array. When addressed with 17 bits of road data, it provides lower and upper 11 bit values for acceptable centroids. This table is not addressed directly by the channel logic but rather via the control logic.

- Test Input: the eighteen bit input to the test FIFO. This FIFO is loaded with simulated SMT data for test purposes.

- Disable: A single bit used to disable all normal functioning of the channel logic. When set, the channel logic reads no SMT or road data and generates no output data.

- Delay: An eight bit word used as the preset count for the delay counter.

- Axial 3/5: A bit used to select either three or five adjacent strips for the axial centroid calculation.

- Stereo 3/5: A bit used to select either three or five adjacent strips for the stereo centroid calculation.

- 90 Degree 3/5: A bit used to select either three or five adjacent strips for the 90 degree centroid calculation.

- Axial Range: Two four-bit chip numbers specifying the first and last chips providing axial data.

- Stereo Range: Two four-bit chip numbers specifying the first and last chips providing stereo data.

- 90 Degree Range: Two four-bit chip numbers specifying the first and last chips providing 90 degree data.

- Axial Threshold #1: The first threshold for axial clustering.

- Axial Threshold #2: The second threshold for axial clustering.

- Stereo Threshold #1: The first threshold for stereo clustering.

- Stereo Threshold #2: The second threshold for stereo clustering.

- 90 Degree Threshold #1: The first threshold for 90 degree clustering.

- 90 Degree Threshold #2: The second threshold for 90 degree clustering.

- Axial dE/dx Threshold #1: dE/dx threshold #1 for axial centroids.

- Axial dE/dx Threshold #2: dE/dx threshold #2 for axial centroids.

- Axial dE/dx Threshold #3: dE/dx threshold #3 for axial centroids.

- Stereo dE/dx Threshold #1: dE/dx threshold #1 for stereo centroids.

- Stereo dE/dx Threshold #2: dE/dx threshold #2 for stereo centroids.

- Stereo dE/dx Threshold #3: dE/dx threshold #3 for stereo centroids.

- 90 Degree dE/dx Threshold #1: dE/dx threshold #1 for 90 degree centroids.

- 90 Degree dE/dx Threshold #2: dE/dx threshold #2 for 90 degree centroids.

- 90 Degree dE/dx Threshold #3: dE/dx threshold #3 for 90 degree centroids.

- HDI ID: Expected HDI ID.

- SEQ ID: Expected SEQ ID.

7.1 Addressing the Road LUT

To reduce the number of address bits needed for downloading the road LUTs, indirect addressing is used via an auto-increment register. The auto-increment register is initially loaded with the LUT starting address (normally zero) by outputting to a particular address in the channel address space. LUT data is then written (read) to a second address, the auto-increment register being incremented after each write (read) operation. The LUT is thus effectively a FIFO when being downloaded.

The control logic rather than the channel logic supplies the 17 bit LUT address but the channel logic controls the 22 bit data and the read and write signals. In normal data processing, the channel logic uses the road write signal from the FRC, ROAD-WR, as the read signal to the LUT, but the address comes from the control logic.
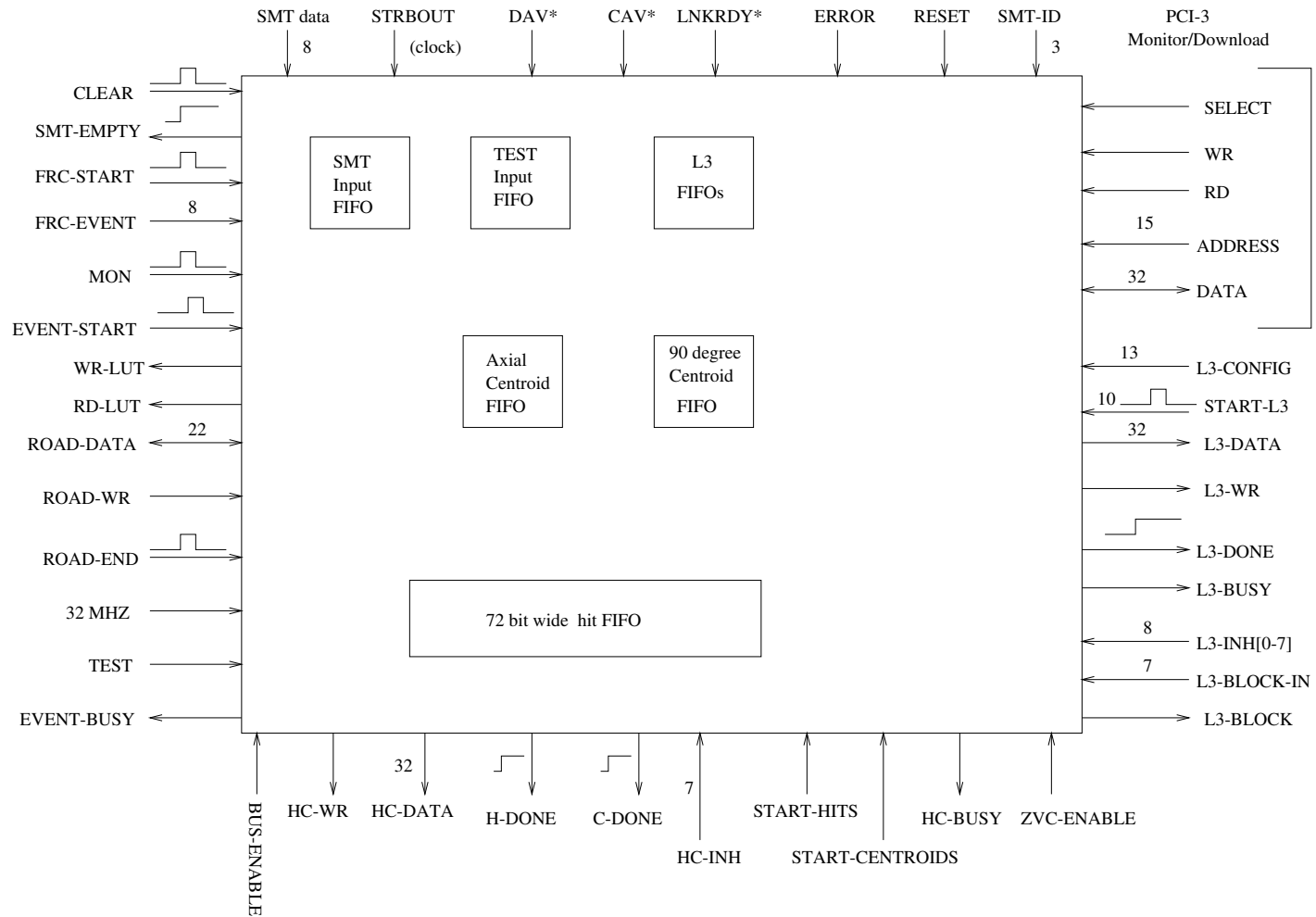
Interface Signals for the Clustering and Hit Filter Logic