Front End Electronics for Particle Detection

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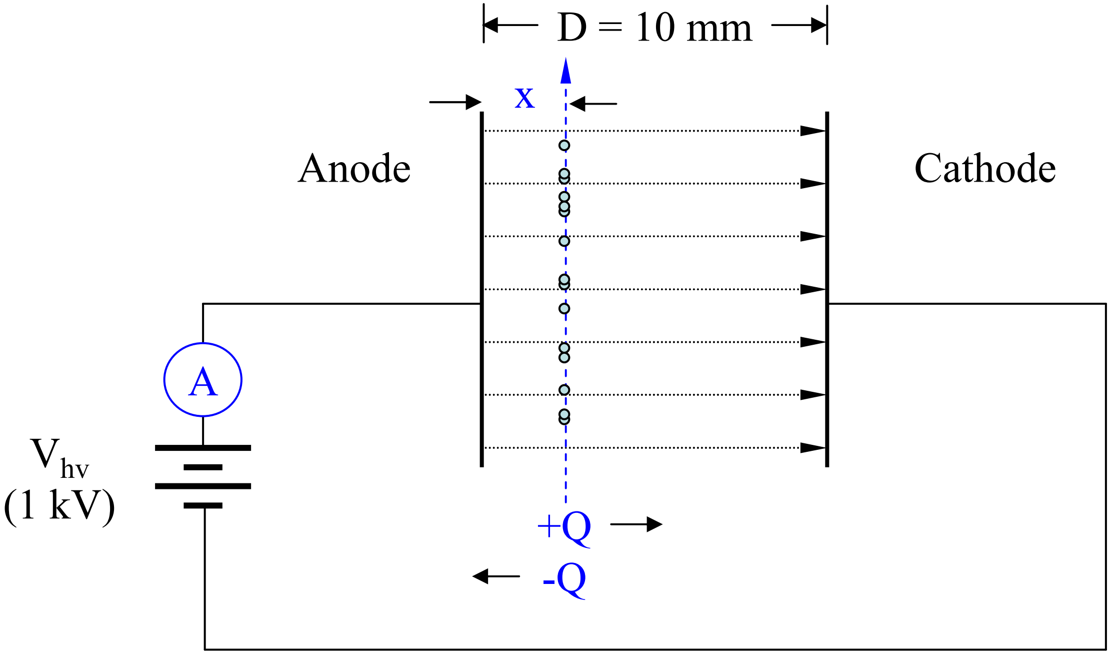
Objectives of front end electronics design

- Understand nature of detector signals
- Identify and understand noise sources in detector and electronic components
- Design signal processing electronics to maximize signal & minimize noise
- Generally one is interested in
  - Total integrated pulse → Calorimeters
  - Pulse "time of arrival" →Spectrometers, tracking detectors
  - Sometimes both.
- Readout of huge number of channels *cheaply* → Take advantage of current ASIC (Application Specific Integrated Circuit) technology

Signal formation in ionization detectors

Simple example : Uniform electric field in drift gas (eg Ar/CO_2)



- Electric field → E = 1e 5 Volts/meter
- Particle track ionizes N electron/ion(Ar) pairs with total charge N*e = Q
- Electrons/ions drift toward Anode/Cathode with velocity given by their mobilities

$$Electrons:\ v_e \approx \mu_e \cdot E \qquad \mu_e \approx 0.4\ \frac{met^2}{V-s}$$

$$Positive\ ions:\ v_{ion} \approx \mu_{ion} \cdot E \qquad \mu_{ion} \approx 6 \cdot 10^{-5}\ \frac{met^2}{V-s} \qquad v_e / v_{ion} \approx 10^4$$

- Question : What signal current i(t) is seen by ideal ammeter in series with battery ?

- Electrons drift to Anode, ions to Cathode
- First the electrons…

In time Δt, electrons move distance $\Delta x = v_e \cdot \Delta t$

through potential $\Delta V = E \cdot v_{drift} \cdot \Delta t$

Work done by field is $\Delta W_{field} = Q \cdot \Delta V$

Work is really done by the battery $\Delta W_{battery} = V_{hv} \cdot i(t) \cdot \Delta t = \Delta W_{field}$

In this example → $\boxed{i(t) = Q \cdot \frac{v_{drift}}{D} = const}$ -------------------- (1)

Total integrated charge collected in arbitrary time t,

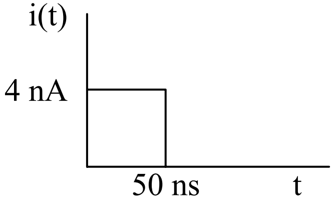
$$\boxed{q(t) = Q \cdot \frac{\Delta V(t)}{V_{hv}} = Q \cdot \frac{x(t)}{D}}$$ -------------------- (2)

Example :

Q = 0.1fc , x = 2 mm (Note: 1fc = 6,250 e)

- electron signal current i(t) = 0.4 nA
- velocity = μE =4*10^4 met/sec
- time to hit anode = 50 ns
- total electron signal charge collected in 50 ns

  q = 0.4 nA * 50 ns = 0.02 fc (~ 125 electrons)



$$\boxed{q(t) = Q \cdot \frac{x}{D} = (2/10) \cdot Q = 0.02\,fc}$$

- What happened to the rest of the ionization charge?
- Need to look at positive ions

$$\boxed{q(t) = Q \cdot \frac{D-x}{D} = (8/10) \cdot Q}$$

→Eventually, we get 100% of the charge, but it takes a *long time* (~ 500 us)

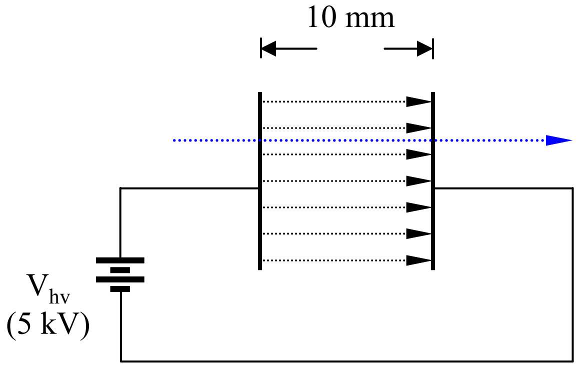
→Summary

- Signal is formed by ***pushing charge through the drift medium***, not by "collecting" it on the anode or cathode.
- Once it hits the electrodes, it no longer contributes.

Variation on the theme
- Liquid Argon Detector (Calorimeter) -

- Liquid argon filled gap, horizontal track
- Large ionization, low velocity
- μ_e = 0.01 met^2/(V-s)   (neglect ion drift)
- Ionization density = 7000 electron-ion pairs per mm of track (MIP) → Much higher than in gas detectors
- Vhv = 5kV
- Total ionized charge 70,000 electrons = ~ 11 fc

→ What does signal current i(t) look like?
→ What's the total charge collected in total electron drift time?



Answer

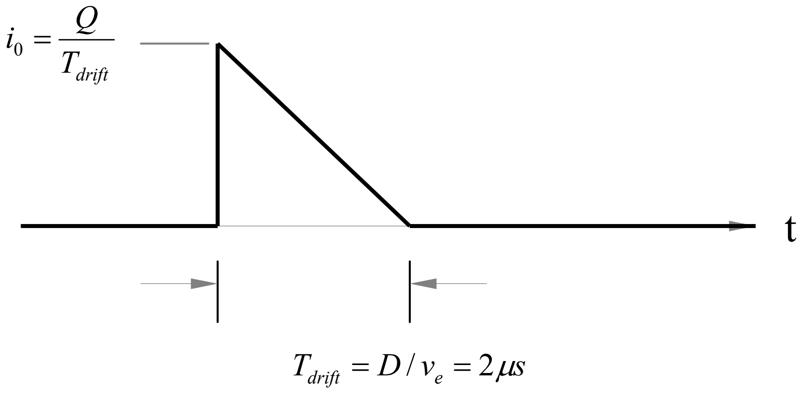
- Divide the track into small segments, Δx, with charge

$$\Delta Q = \frac{\Delta x}{D} \cdot Q$$

- Each segment contributes identical current until it disappears into electrode

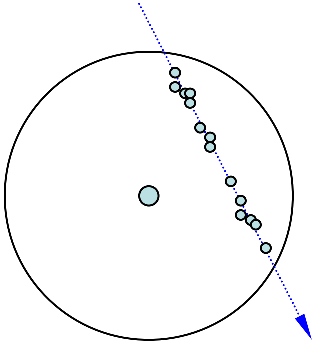
$$\Delta i = \frac{\Delta Q \cdot v_e}{D}$$

- Add up all the segments



- Total integrated charge? → Q/2

Signals in circular drift tube or wire chamber



- Electric field → $$E(r) = \frac{1}{r} \cdot \frac{V_{hv}}{\ln(R / r_0)}$$ -------------------- (3)
- Primary electrons drift to Anode wire.
- High field at wire surface causes avalanche “centered” very close to wire
- Each primary electron liberates many secondary electrons → Gas gain ($10^3 - 10^5$)
- Timing measurement gives radial position of track.
- Must analyze both electron and ion signal response to single primary electron

Electron signal

- Charge centroid *very* close to wire → very short collection time , < 1 ns
- Electrons quickly disappear into the anode → Electron signal generally can be neglected.

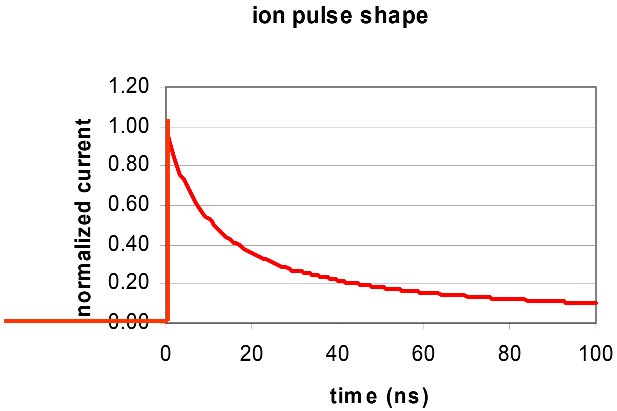
Positive ion signal

- Ion velocity follows electric field resulting in;

$$\boxed{i(t) = Q \cdot const \cdot \frac{t_0}{t + t_0}}$$

where the two constants are functions of detector parameters such as mobilities, gas gain, wire and tube diameters, etc. (Details in NEPPSR-II)

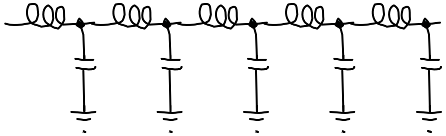
- Typical wire chamber t_0 ~ 1ns – 20ns
- For ATLAS Muon Spectrometer, t_0=11ns
- This signal has very long “positive ion tail”



- For use as a position sensitive detector, one is generally interested only in the first few tens of ns of the signal.
- Integrated charge increases only logarithmically.
- Integrated charge in time t_0 is only about 5% of total
- ATLAS-MDT : Ggain=2e4 → “Effective” charge gain ~ 1,000

Basic passive components and noise sources

- **Inductor**
  - Stores energy in magnetic field
  - $E = \frac{1}{2} L i^2$
  - Impedance $Z(\omega) = j\omega L$
  - Lossless, noiseless
- **Capacitor**
  - Stores energy in electric field
  - E = ½ C v2
  - Impedance $Z(\omega) = 1/(j\omega C)$
  - Lossless, noiseless
- **Ideal transmission line (cable)**
  - Considered as infinite sequence of series inductors & parallel capacitors



  - Results in wave equation with phase velocity

$$v = \frac{1}{\sqrt{\varepsilon \cdot \mu}}$$

  - and a constraint between voltage and current :

$$\frac{V}{I} = \sqrt{\frac{\mu}{\varepsilon}} = Z_0 \ \textit{characteristic impedance}$$

  - noiseless
  - Note that an infinitely long transmission line is indistinguishable from a resistor of value Z_0
  - As corollary, a finite line with a resistor of value Z_0 at its end, is also indistinguishable from a resistor of value Z_0.
  - In other words, if you launch a pulse into a terminated line, it never comes back (no reflection).

- **Resistor**
  - ➢ Electric field pushes conduction electrons through a lattice
  - ➢ Dissipates power = I*V
  - ➢ Conduction electrons (generally) in thermal equilibrium with environment
  - ➢ Noisy → Noise characterized by “noise power density” p(f) [watts/hz]

$$p(f)\cdot df \equiv power\,(watts)\ in\ frequency\,range\ f\ to\ f+df$$

  - ➢ p(f) is frequently expressed as a voltage density (in series) or current density (in parallel)

$$p(f)=\frac{e_n^{\,2}(f)}{R} \qquad\qquad p(f)=i_n^{\,2}(f)\cdot R$$

  - ➢ e_n(f) & i_n(f) given in volts/sqrt(hz) & amps/sqrt(hz)
  - ➢ To get values of e_n(f) & i_n(f) ; [Nyquist, Phys Rev, Vol 32, 1928, p. 110]
  - ➢ Result follows directly from equipartition theorem → “Thermal noise”

$$\boxed{\begin{aligned}&p(f)=4\cdot k\cdot T\\&or\ \ equivalently\\&i_n=\sqrt{\frac{4\cdot k\cdot T}{R}}\\&\&\\&e_n=\sqrt{4\cdot k\cdot T\cdot R}\end{aligned}}$$

Notes:

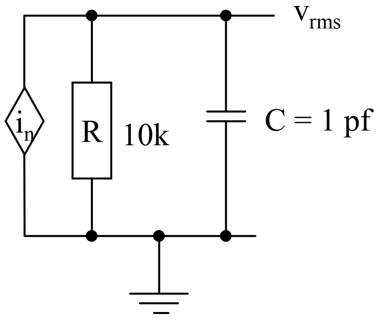
- For a resistor i_n & e_n are independent of frequency → “White” noise source.
- All frequency components are considered uncorrelated.

AC Circuit analysis

- Same as DC except use complex impedances for Ls and Cs
- Typically calculate output/input (Transfer function) in freq domain.
- Inverse Fourier (or Laplace) transforms get you to the time domain

"kT/C" noise

What is the rms terminal voltage of the following simple circuit?



Solution

1) **Add noise current density,** $i_n = \sqrt{\dfrac{4kT}{R}}$

2) **Solve for circuit "transfer function" (v/i) →** This gives you output voltage *density*

$$v_n(\omega) = \frac{R}{1 + j \cdot \omega \cdot R \cdot C} \cdot i_n$$

- set $\omega = 2\pi f$

3) **Integrate over frequencies (quadrature)**

$$v_{rms}^2 = \int_0^\infty |\, v_n^2(f) \,| \cdot df = \frac{4 \cdot k \cdot T}{R} \cdot \frac{1}{2 \cdot \pi} \cdot \int_0^\infty \frac{R^2}{(1 + R^2 \cdot C^2 \cdot \omega^2)} \cdot d\omega$$

$$v_{rms}^2 = \frac{4 \cdot k \cdot T}{C} \cdot \frac{1}{2 \cdot \pi} \cdot \int_0^\infty \frac{1}{(1 + x^2)} dx \qquad \textit{where} \;\; x = \omega \cdot RC$$

- In general, such integrals can be *looked up* (or done by *contour integration for those who like to suffer).*

$$\int_0^\infty \frac{1}{(1 + x^2)} dx = \frac{\pi}{2}$$

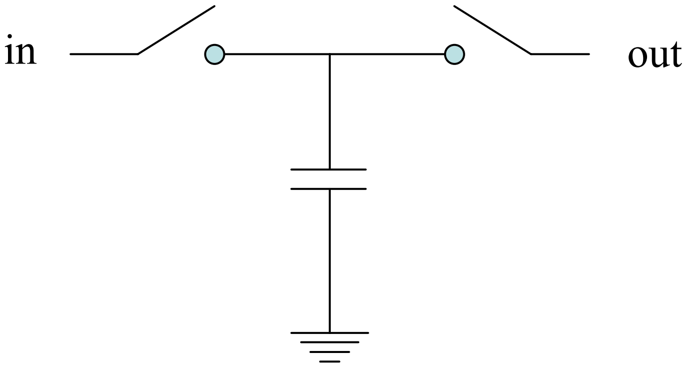
- In this case,

$$v_{rms} = \sqrt{\frac{kT}{C}}$$

- Note that it is independent of resistance, R
- At room temperature kT ~ 4e-21 →

$$V_{rms} = 63\mu V$$

- Question : Why do we care about this? Where does it show up?
- Consider a “Sample & Hold” circuit. We charge up a capacitor through a “switch” to a given voltage, then open the switch.
- The capacitor “remembers” the voltage forever.
- Close the second switch to “read” the S/H cell.



- A realistic switch is frequently a semi-conductor device with finite resistance
- Repeated charging and reading results in rms error of kT/C
- Example: If total signal range is ~ 2V (common these days) → SNR ~ 32,000 or 15 bits dynamic range →

For high dynamic range, you want a big capacitor (Sometimes hard to come by in integrated circuits)

Shot noise

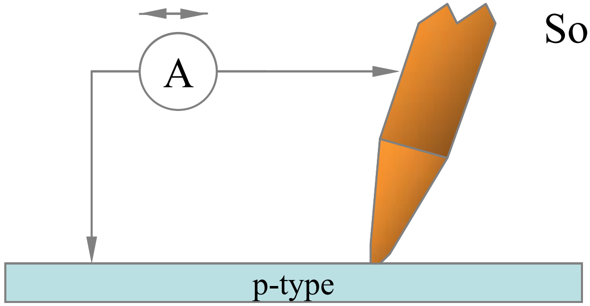
- Important when (small) currents must overcome a *barrier*
- Results from discrete nature of current → carried by electrons of charge q_e
- Movement of small electric currents is governed by Poisson statistics
  - ➢ Current : $I = R_e \times q_e$ ([R_e] electrons/sec)
  - ➢ In time ΔT, $N_e = R_e \times \Delta T$ cross the barrier
  - ➢ Fluctuation in that number = sqrt(N_e)
- This is equivalent to a *noise current density* given by

$$i_n = \sqrt{2 \cdot I \cdot q_e} \quad amps/rt(Hz)$$

- Independent of temperature
- Generally caused by detector or electronic leakage currents (which generally are temperature dependent)
- May often be a dominant detector noise source

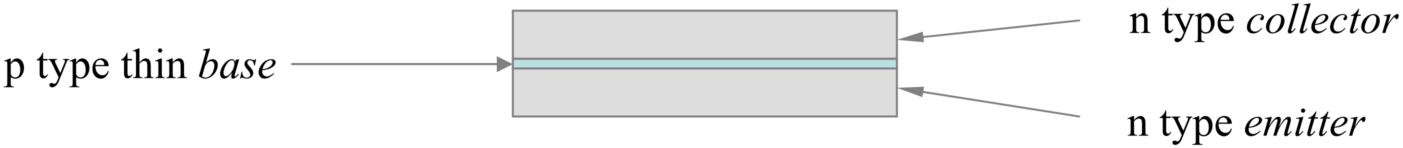
Semiconductor devices

- Rely on two distinct types of charge carriers → Electrons & holes
- Intrinsic semiconductor – Lattice of atoms (eg silicon) with complete valence locations (4) filled → 4 covalent bonds per site
- N-type semiconductor (eg n-doped silicon, dopant has 5 valence electrons) has excess electrons for conduction
- P-type (eg p-doped silicon, dopant has 3 valence electrons) has dearth of electrons
- Missing electrons in lattice behave as positively charged carriers → holes
- Question : Are holes "real" or just a nice way of thinking about missing electrons?
  - Ans: They're real. → They carry heat as well as current so we can observe heat flow (and current flow) with an ammeter. (Also verified by Hall effect)



Soldering iron

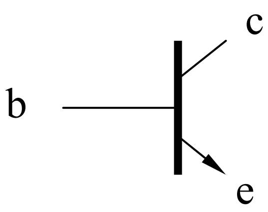
Active electronic devices
Bipolar Junction Transistors (BJT)
(Bardeen, Brattain, & Shockley – 1947)



p type thin *base*

n type *collector*

n type *emitter*

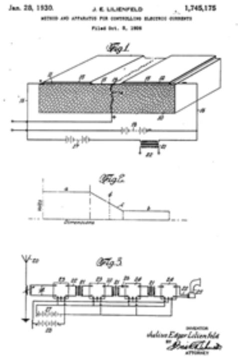


Features

- be junction forward biased → Like diode in on-condition →causes lots of current flow
- cb junction is reverse biased (like diode in off condition)
- But base is thin so *emitted* current goes through and is collected by *collector*
- Base only needs to supply current lost to recombination. → Device has current gain ~ 100
- All active semiconductor devices characterized by *transconductance* (gm) → Ratio of change in collector current per unit change in be voltage.
- BJT has large gm per unit collector current → q_e/kT =~ 40 amps/volt at room temp

BJT Features (con't)

- BJT has very large g_m per unit collector current → q_e/kT =~ 40 amps/volt at room temp (This is good! → High gain at low power.)
- Used extensively for discrete designs (< 1980s)
- Can be integrated into Application Specific Integrated Circuits (ASICs)
- Processing is expensive & time consuming. Several $100k / run in 1990s
- Until 1990's BJT were primary building blocks for high speed circuits

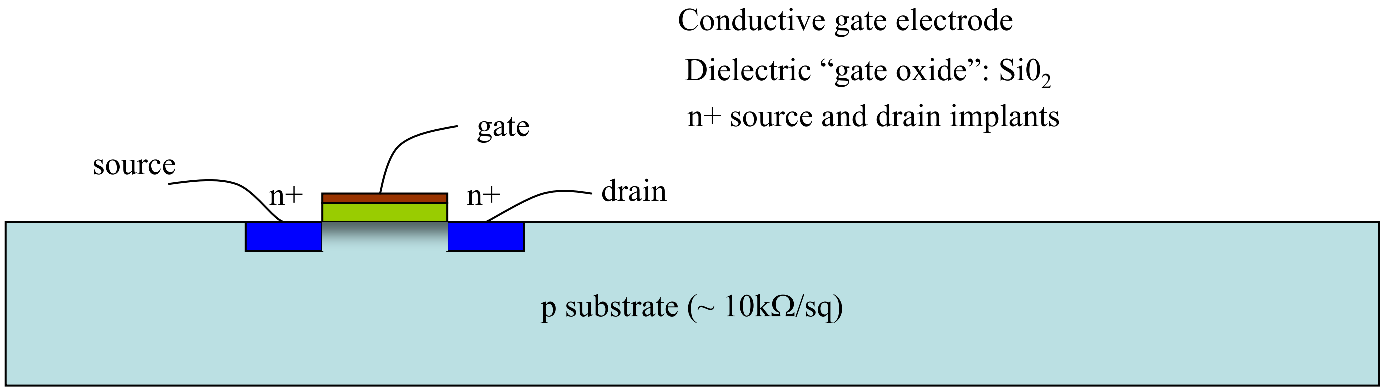


Field Effect Transistors

- Patented in 1928 by J. Lilienfeld ("Transfer Resistor")
- Alas, soon forgotten, revived in the 1950's
- CMOS logic ICs appears in 60's & 70's
- Geometries shrink rapidly (Moore's law)
- Speed improves with shrinking geometry
- Early '90s → Viable for analog integrated circuits at "gate length" ~ 1um
- Currently at 0.065 um and falling.
- Presently has replaced BJTs for most logic & microprocessors, and many analog applications.
- fet vs bjt ratio in known universe >>> 1 zillion

CMOS components : Field effect transistors (nfets)

- In undoped (intrinsic) silicon, electron and hole densities are the same (thermal only)
- n-doped (arsenic, phosphorous, antimony,..) : electron density increases, hole density decreases
- p-doped (boron, aluminum, gallium, ..) : vice-versa
  - Strength of doping denoted by + sign → n, n+, p, p+
  - \+ sign indicates higher doping, lower resistivity



- With Vgate = 0, structure is non-conductive (back to back diodes)
- Increasing Vgate in positive direction, attracts *electrons* from substrate
- When Vgate > Vthreshold, “channel” becomes conductive. Conductance increases as Vgate increases.
- As Vdrain is made more positive than Vsource, current starts to flow
- Voltage gradient appears from drain to source.
- Electric field is strongest near source, weakest near drain..

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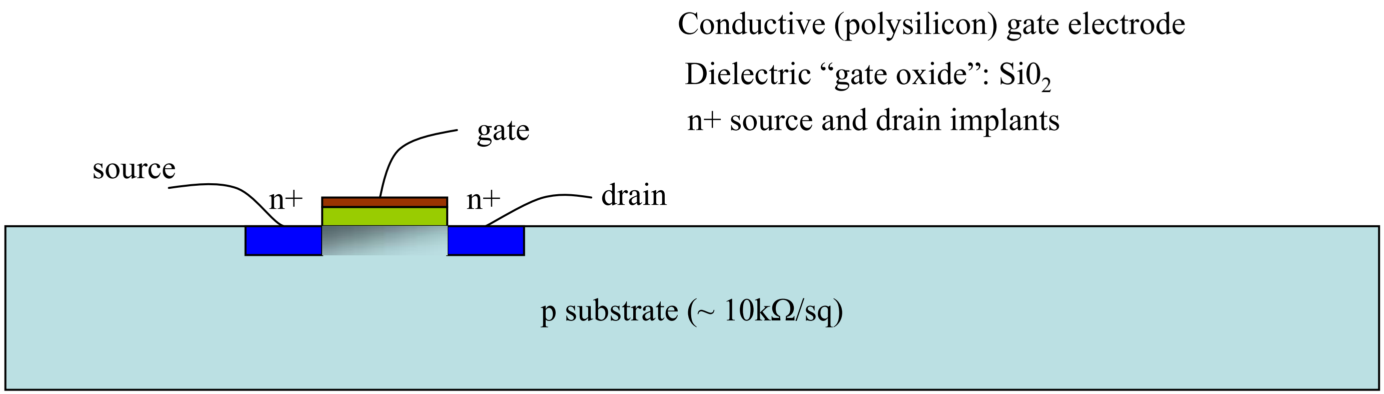

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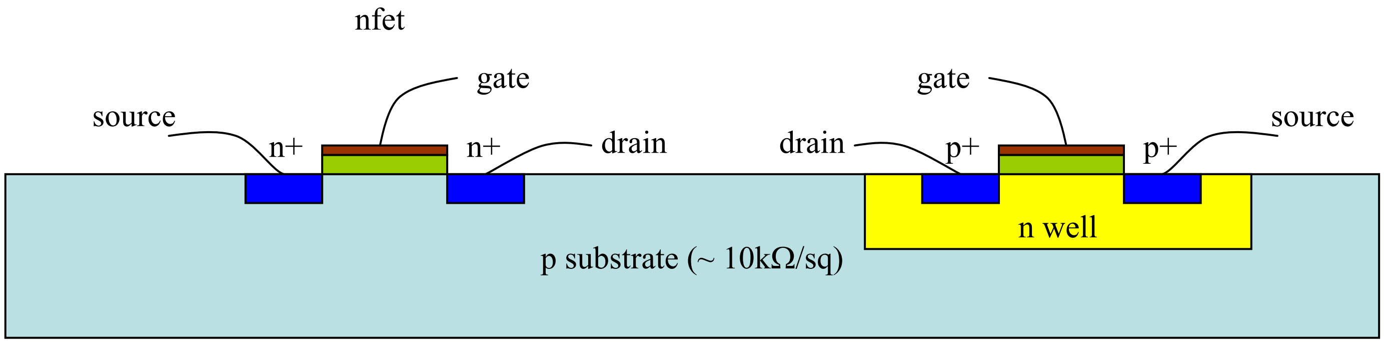
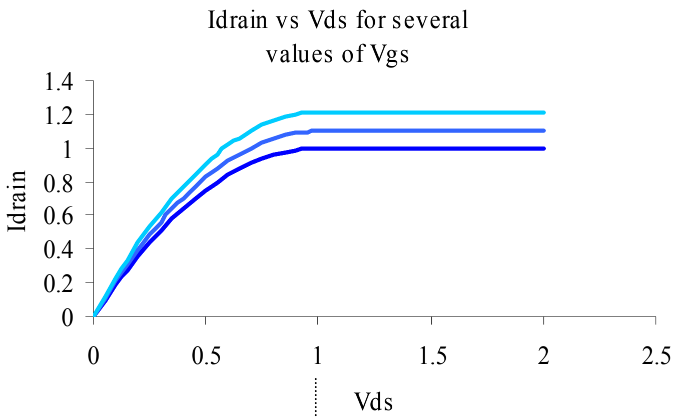
- As Vdrain is made more positive than Vsource, current starts to flow
- Voltage gradient appears from drain to source.
- Electric field is strongest near source, weakest near drain.
- Channel charge density “tilts” toward source.
- Drain current increases with Vdrain
- When Vdrain comes within a “threshold voltage” of Vgate, (Vdrain = Vgate – Vthreshold) current “saturates”
- Saturation region also called “pinch-off

CMOS components : Field effect transistors
pfets



- Generally, pfet drain current constant, Kp, is about 1/3 that of nfets due to lower hole mobility
- For same size transistor at same current, pfet transconductance is smaller by ~sqrt(3)

FET properties (simplified model)



Linear, resistor, or triode region

“Saturation” region

Drain current properties in saturation region

- Id increases quadradically with Vgs

$$I_d \propto (V_{gs} - V_{th})^2$$

- Increases linearly with transistor channel width, W
- Decreases linearly with transistor gate length, L

$$I_d \equiv \frac{1}{2} \cdot K_n \cdot \frac{W}{L} \cdot (V_{gs} - V_{th})^2 \qquad \text{----------------------------- (13)}$$

- Definition: “Transconductance” = ratio of change in drain current per unit change in gate voltage.

$$g_m = \frac{\partial I_d}{\partial V_{gs}} = \sqrt{2 \cdot I_d \cdot K_n \cdot \frac{W}{L}} \qquad \text{----------------------------- (14)}$$

$$"Typical"\, value: K_n \approx 100 \mu A / V^2$$

FET properties (con't)

Terminal "impedances"

- Gate: No dc current flow, just gate capacitance Cgate (of order ~tens of femtofarads to pf)
- Drain:
  - "Wiggle" the drain voltage a little, what's the change in drain current?
  - Ans: none (or very little) change so →

$$Z_{drain} \equiv \frac{\partial V_{ds}}{\partial I_d} \approx \infty$$

- Source
  - "Wiggle" the source voltage a little bit.
  - This changes Vgs and thus drain current (and source current) by (Vgs) x (g_m).

$$Z_s \equiv \frac{\partial V_s}{\partial I_d} \approx \frac{1}{g_m}$$

  - Typical numbers depending on application;

$$.001 > g_m > .01$$

$$or$$

$$1k\Omega < Z_{source} < 100\Omega$$

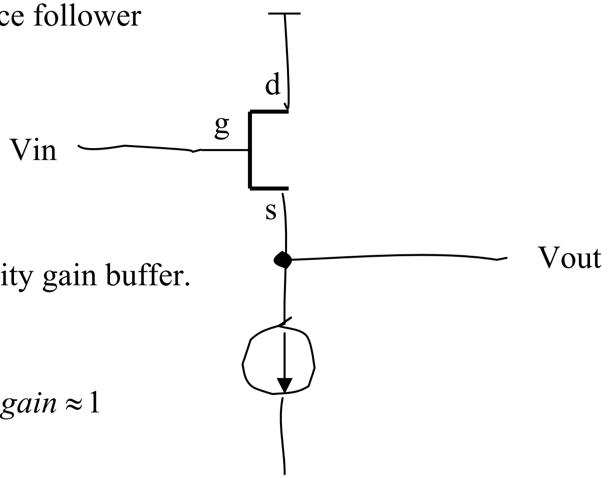
  - Example;
    - Idrain = 1 ma, L=0.5u, W=100u

$$g_m = \sqrt{2 \cdot I_d \cdot K_n \cdot \frac{W}{L}} = \sqrt{2 \cdot (10^{-3}) \cdot (100 \cdot 10^{-6}) \cdot 200} = 6.3 \cdot 10^{-3}$$

$$or \qquad Z_s \approx 160\Omega$$

Some simple FET circuits

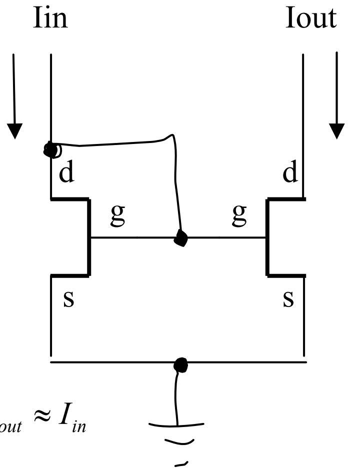
A) Source follower



Used as (almost) unity gain buffer.
Hi-Z in, Lo-Z out.

$Voltage\ gain \approx 1$

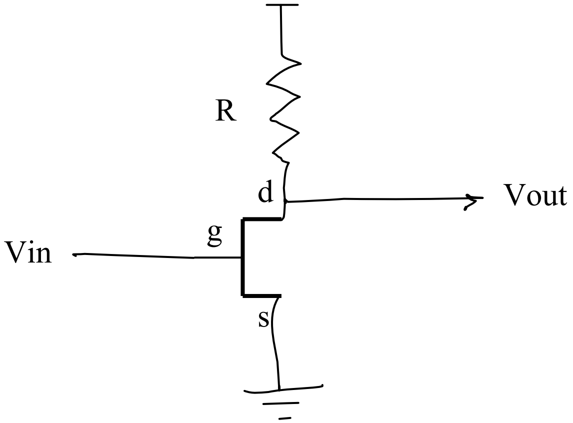
C) Current mirror



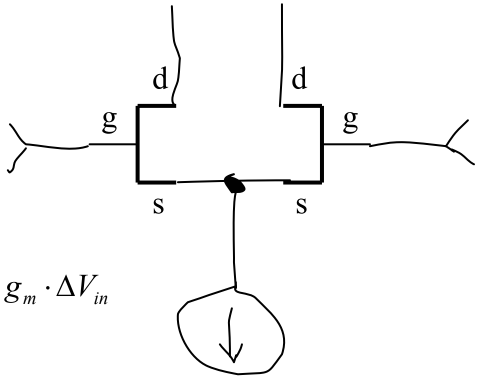
$I_{out} \approx I_{in}$

B) Common source amplifier

$Gain = g_m \cdot R_{load}$



D) Differential amplifier

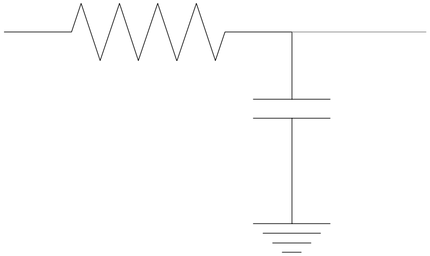


$\Delta I_{out} = g_m \cdot \Delta V_{in}$

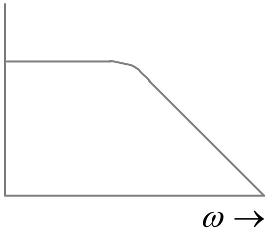
Shaping

- Use of RC and active circuits to
  - ➢ produce useful pulse shapes
  - ➢ maximize response to detector signal
  - ➢ minimize response to noise
  - ➢ avoid “pile-up” or baseline drift due to rapid arrival of signals (as in “hot” areas of detectors)
- Useful to analyze in both frequency and time domains
- Examples:

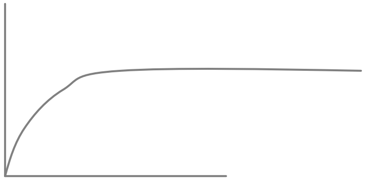
Low pass filter (integrator)



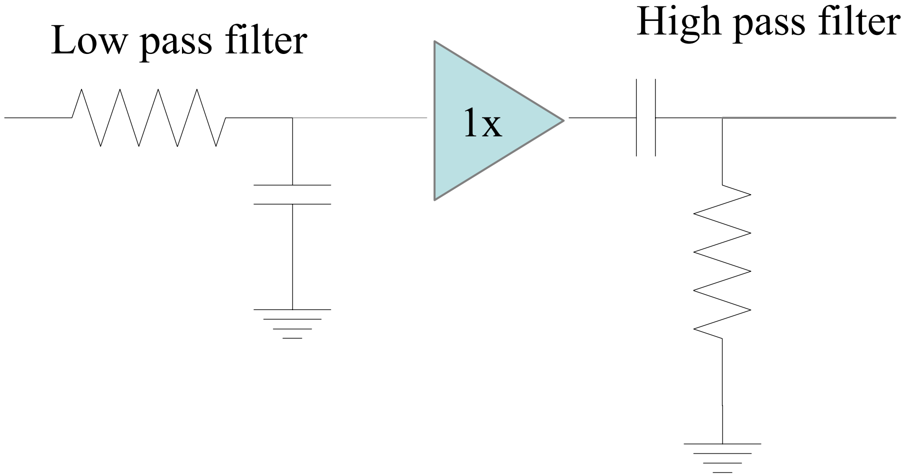
Freq



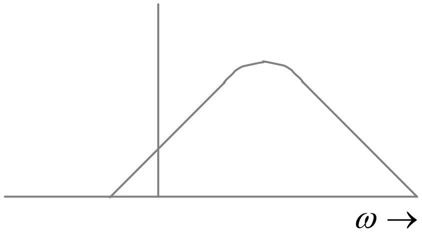
Step response



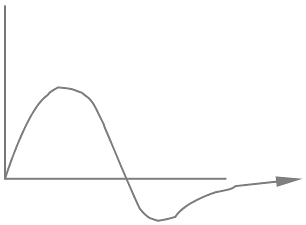
“RC-CR” shaper



Freq response

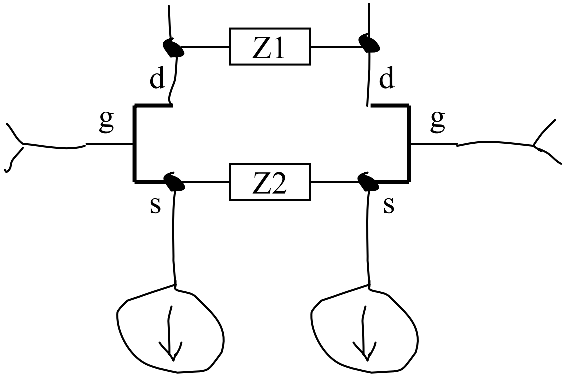


Step response – “bipolar” shaper

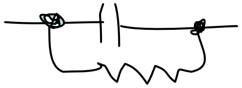


Some common FET gain & shaping circuits – con't

E) Fancier differential amplifier



- "Boxes" Z1 & Z2 can be whatever you need
- example:
  - Z_1 is parallel RC



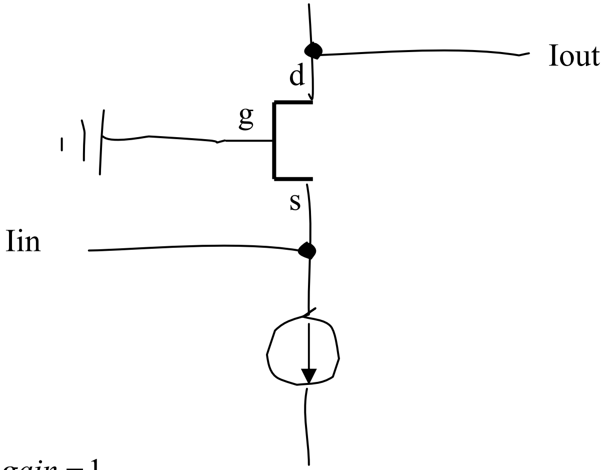
  - Z_2 is series RC

- Transfer function is

$$H(s) \approx \frac{Z_1(s)}{Z_2(s)} = \frac{sRC}{(1+sRC)^2} \qquad where\ s \equiv j \cdot \omega$$

→ Implements a "Bipolar" shaping function with gain

F) Common gate or "cascode"



$Current\ gain = 1$

Used as current buffer.
Lo-Z in, Hi-Z out.

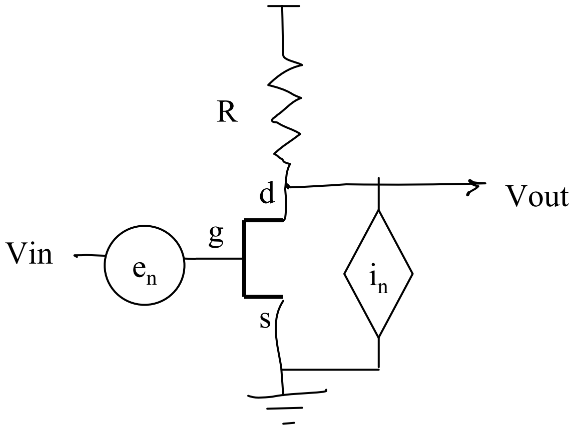
Noise in Fets

- Fet channel is resistive and will thus have a thermal noise current component, i_n

$$i_n \propto \sqrt{\frac{4 \cdot k \cdot T}{R_{effective}}} \propto \sqrt{4 \cdot k \cdot T \cdot g_m}$$

- Channel is not a single resistor, but rather a series of increasing resistances (from source to drain)
- A fudge factor will be needed! (ff = 2/3)

$$i_n = \sqrt{\frac{8}{3} \cdot k \cdot T \cdot g_m}$$



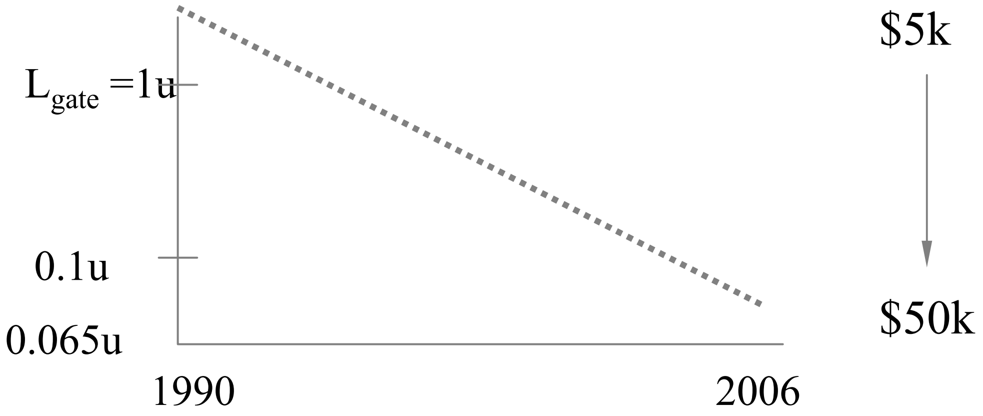
- Noise current in drain is equivalent to noise voltage in gate with $e_n = \dfrac{i_n}{g_m}$

$$e_n = \sqrt{\frac{8}{3} \cdot \frac{k \cdot T}{g_m}} \qquad \text{----------------------------- (15)}$$

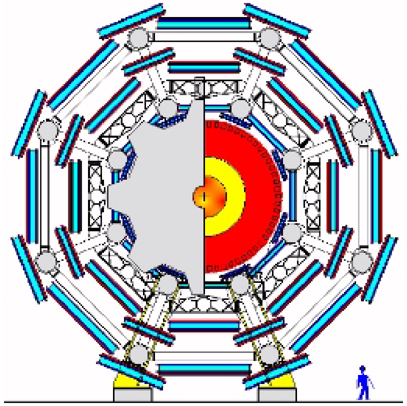
- For low noise → High gm , very wide transistor, fairly large current

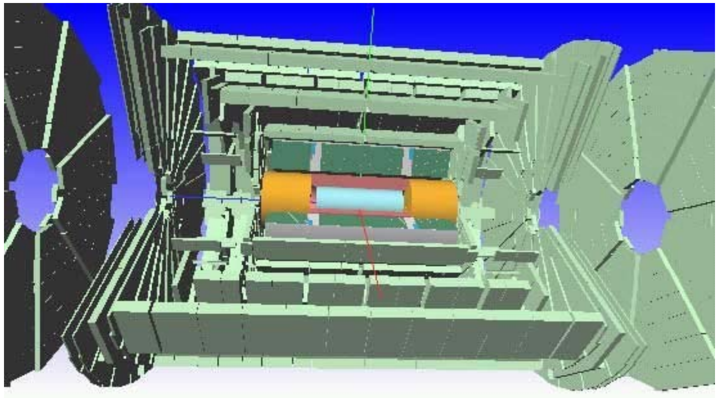
Access to CMOS technologies

- Commercial foundries are interested in manufacturing runs of order >> 10^6 chips per run (eg microprocessors, logic chips)
- HEP requirements ~ $10^4 – 10^5$ chips/experiment → very small users
- We need a “broker” → MOSIS
  - → Metal Oxide Semiconductor Integration Service
  - → Provides detailed transistor models for simulations (SPICE)
  - → Sells “real estate” on integrated circuit manufacturing to many customers
  - → Submits a collection of designs to vendors (who don’t care what the design function is) : Multi-Project Wafer (MPW) →HP, IBM, TSMC, AMS, ……
  - → Returns prototype parts to customer for reasonable cost ($5k - $50k)



Example : ATLAS Muon Spectrometer



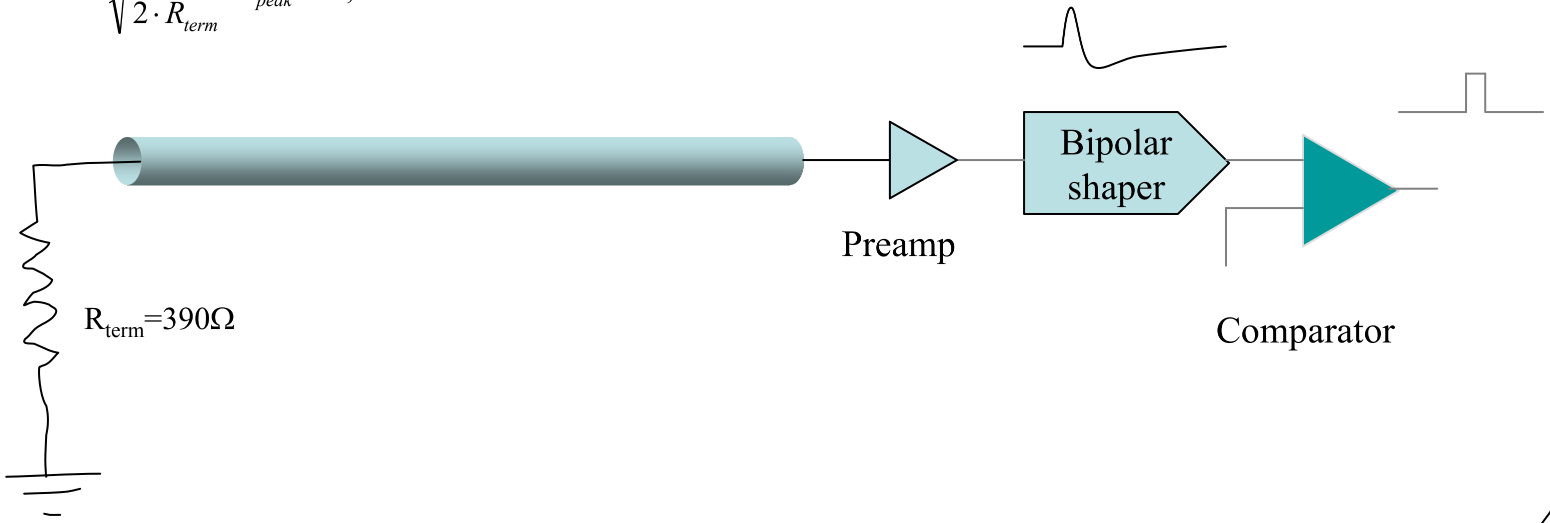


- ~350,000 circular “Monitored Drift Tubes (MDTs)
- ~ 1,000 chambers
- Wire radius : r_0=25 microns
- Tube radius : R= 15 mm
- Gas : Ar/C02 (93%/7%)
- V_{hv} = 3080 Volts
- Gas gain: G = 2e4
- μ_{ion} = 6e-5 m^2/V-s
- μ_e = 0.4 m^2/V-s
- Tube length up to 6 meters
- $Z_0 \sim 390\ \Omega$

Objectives

- MDTs are “position” detectors for particle momentum measurement (curvature in B field)
- Target resolution ~ 80 u per single tube
- Need to measure “time of arrival” of pulse to ~ 1 ns
- Strategy
  - ➢Form pulse with short (~ 15ns) peaking time
  - ➢ Measure time that pulse exceeds fixed threshold
- To avoid pulse reflections, we need a “terminating” resistor
- Terminating resistor sets lower limit on noise (follows from “noise integrals” see pg 11)

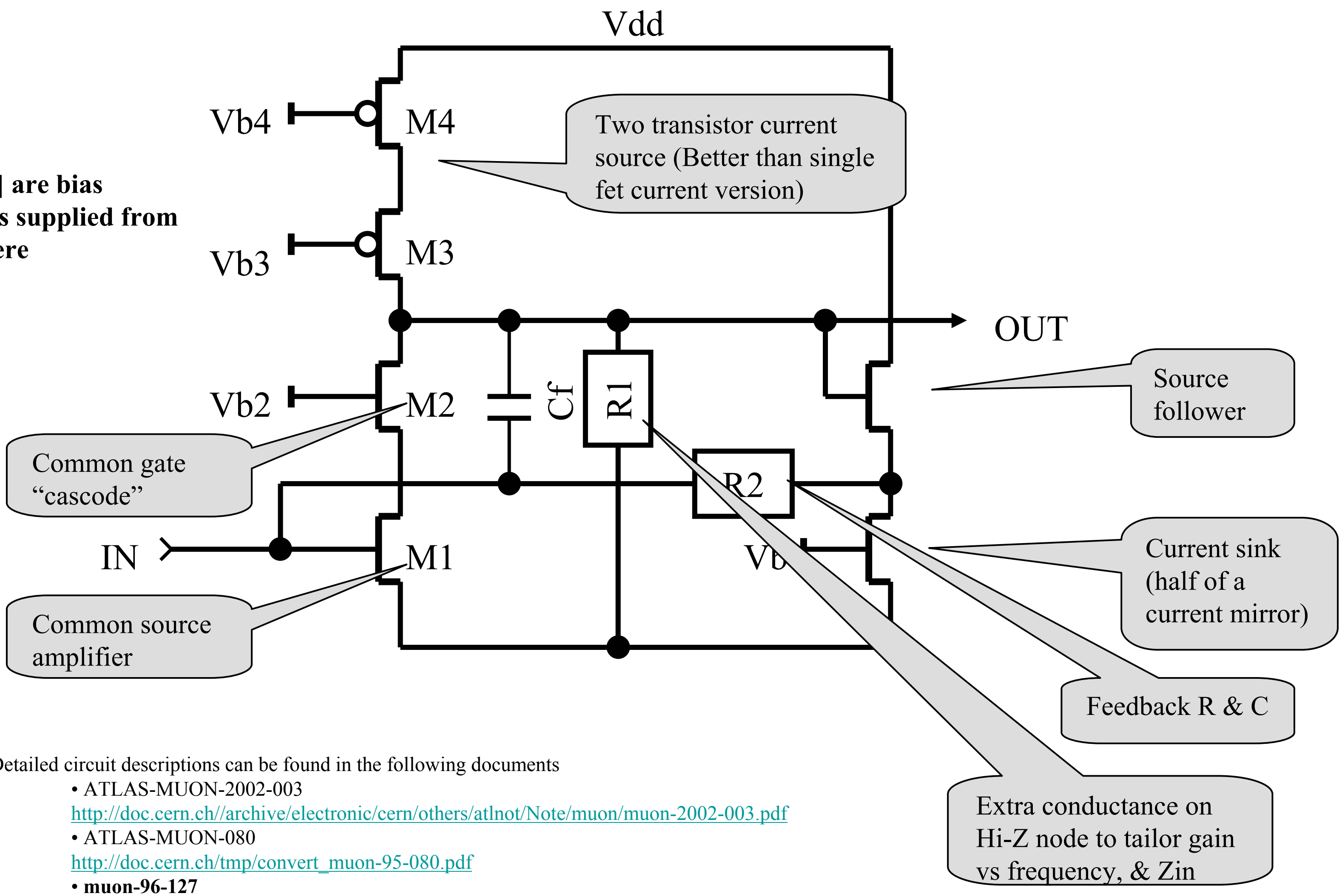
$$enc = e^1 \cdot \sqrt{\frac{kT}{2 \cdot R_{term}} \cdot T_{peak}} \approx 5{,}000 \ electrons\, rms$$



MDT-ASD topology

Preamplifier

Vb[1:4] are bias voltages supplied from elsewhere



Two transistor current source (Better than single fet current version)

Source follower

Common gate “cascode”

Current sink (half of a current mirror)

Common source amplifier

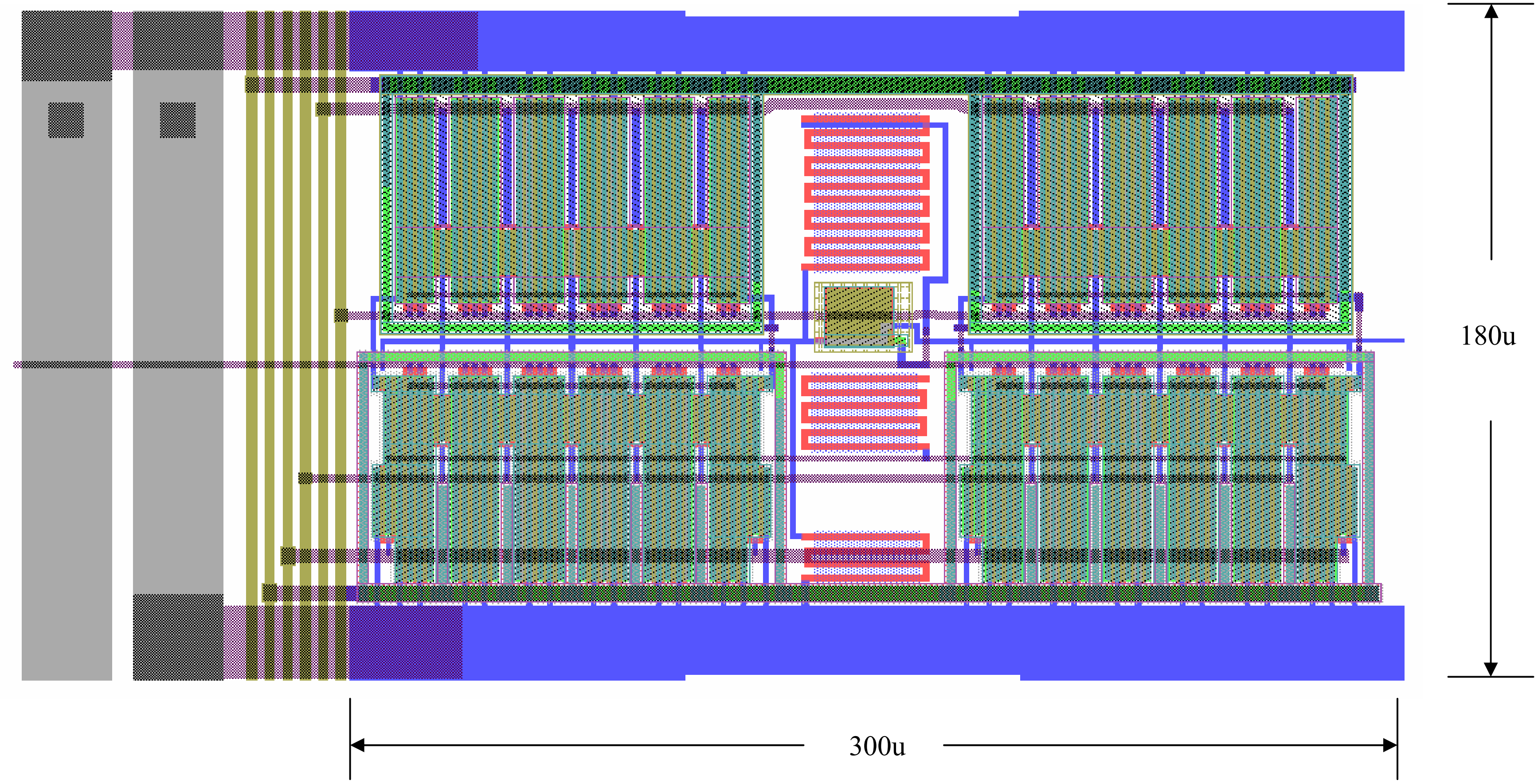
Feedback R & C

Extra conductance on Hi-Z node to tailor gain vs frequency, & Zin

Detailed circuit descriptions can be found in the following documents

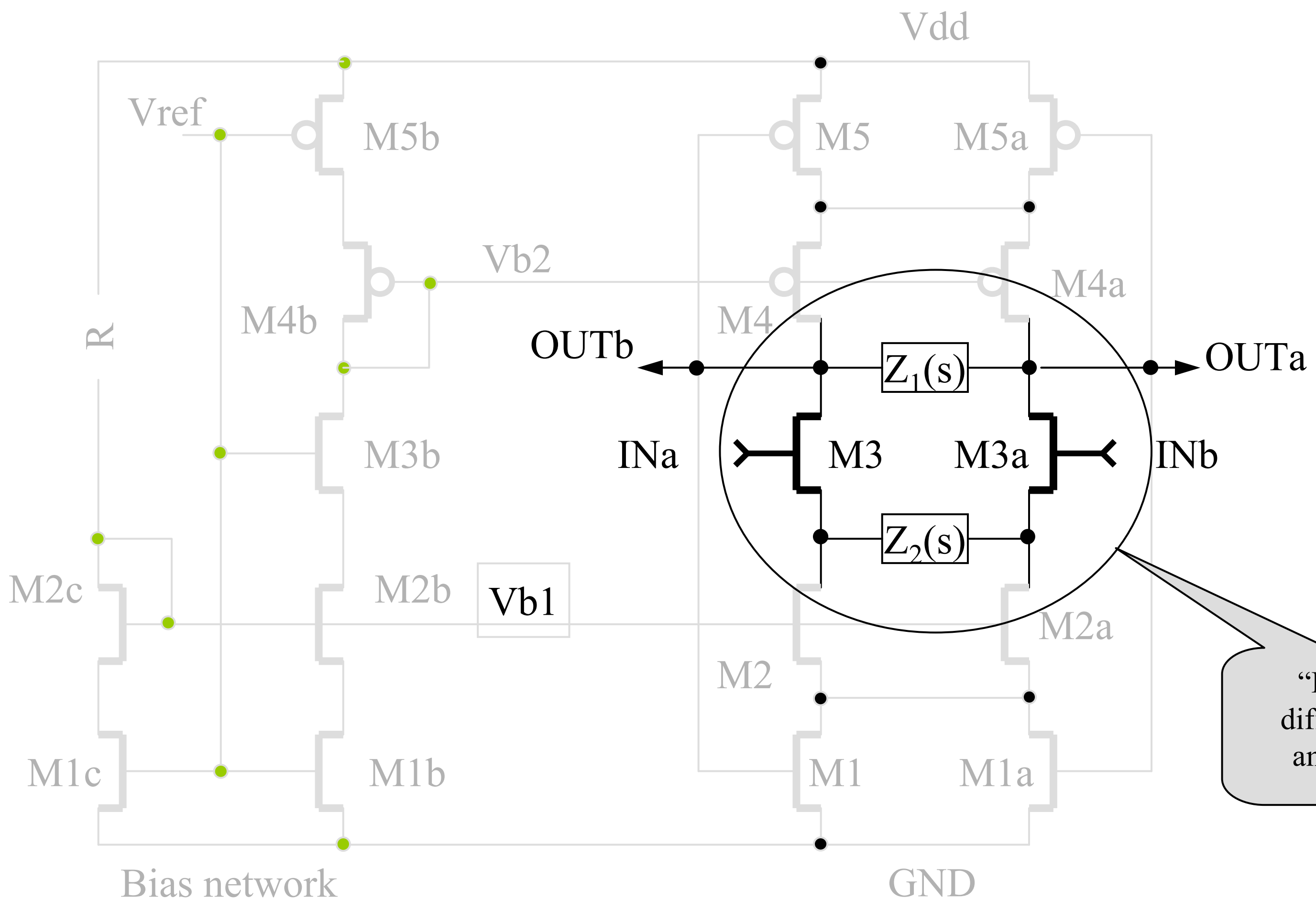
- ATLAS-MUON-2002-003
  http://doc.cern.ch//archive/electronic/cern/others/atlnot/Note/muon/muon-2002-003.pdf
- ATLAS-MUON-080
  http://doc.cern.ch/tmp/convert_muon-95-080.pdf
- **muon-96-127**
  http://doc.cern.ch/cgi-bin/extractFigs.check.sh?check=/archive/electronic/cern/others/atlnot/Note/muon/muon-96-127.ps.gz

MDT-ASD preamp layout



MDT-ASD topology

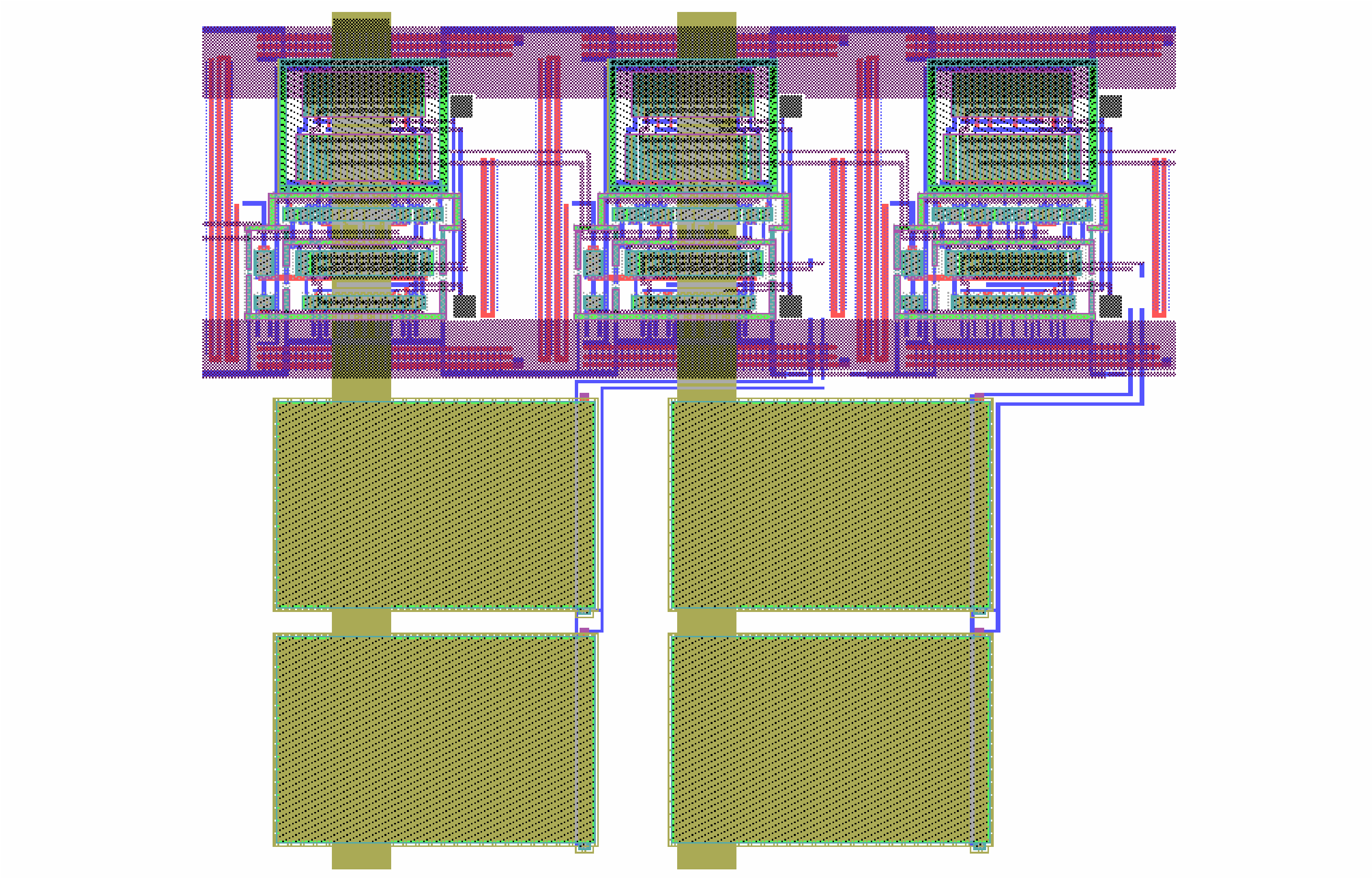
Shaper differential amplifiers



"Fancy" differential amplifier

MDT-ASD topology

Shaper differential amplifiers



ATLAS MDT-ASD Summary

- Design resulted in octal “MDT-ASD” chip (Amp/Shaper/Discriminator”
- HP 0.5 u CMOS process (now considered very “20th century” process)
- 75k chips produced & tested
- ~ 50k chips used in ATLAS
- Cost ~ $1/channel
- 3 MDT-ASD chips per “MDT Mezzanine” card
- ~ 16,000 “Mezz” cards produced and now in ATLAS Muon Spectrometer

Summary & conclusions

Analysis/design methodology

1. Understand requirements
    - Noise, dynamic range,..
    - Impedances
    - Signal shapes
    - etc
2. Hand calculations will get you close and/or guide design
    - Noise contributions of worst offenders
    - Transfer functions, response shapes, etc
    - Transistor sizing for CMOS circuits
3. SPICE modeling
    - Vendor SPICE models can be very accurate but very complicated
    - Produce best analysis at expense of intuitive understanding

Moore's law

- Number of transistors on a single die will double every ~18 months (G. Moore)
- Corollary → Complexity and channel count of HEP experiments scales about the same way – It's not an accident.

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4) "Electronics for the Physicist" Delaney, Halsted Press
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7) "Processing the signals from solid state detectors" Gatti & Manfredi, Nuovo Cimento
8) "Analog MOS Integrated Circuits for Signal Processing" Gregorian & Temes, Wiley Interscience
9) "Detector Physics of the ATLAS Precision Muon Chambers" Viehhauser, PhD thesis, Technical University Vienna.
10) "MDT Performance in a High Rate Background Environment" Aleksa, Deile, Hessey, Riegler – ATLAS internal note, 1998