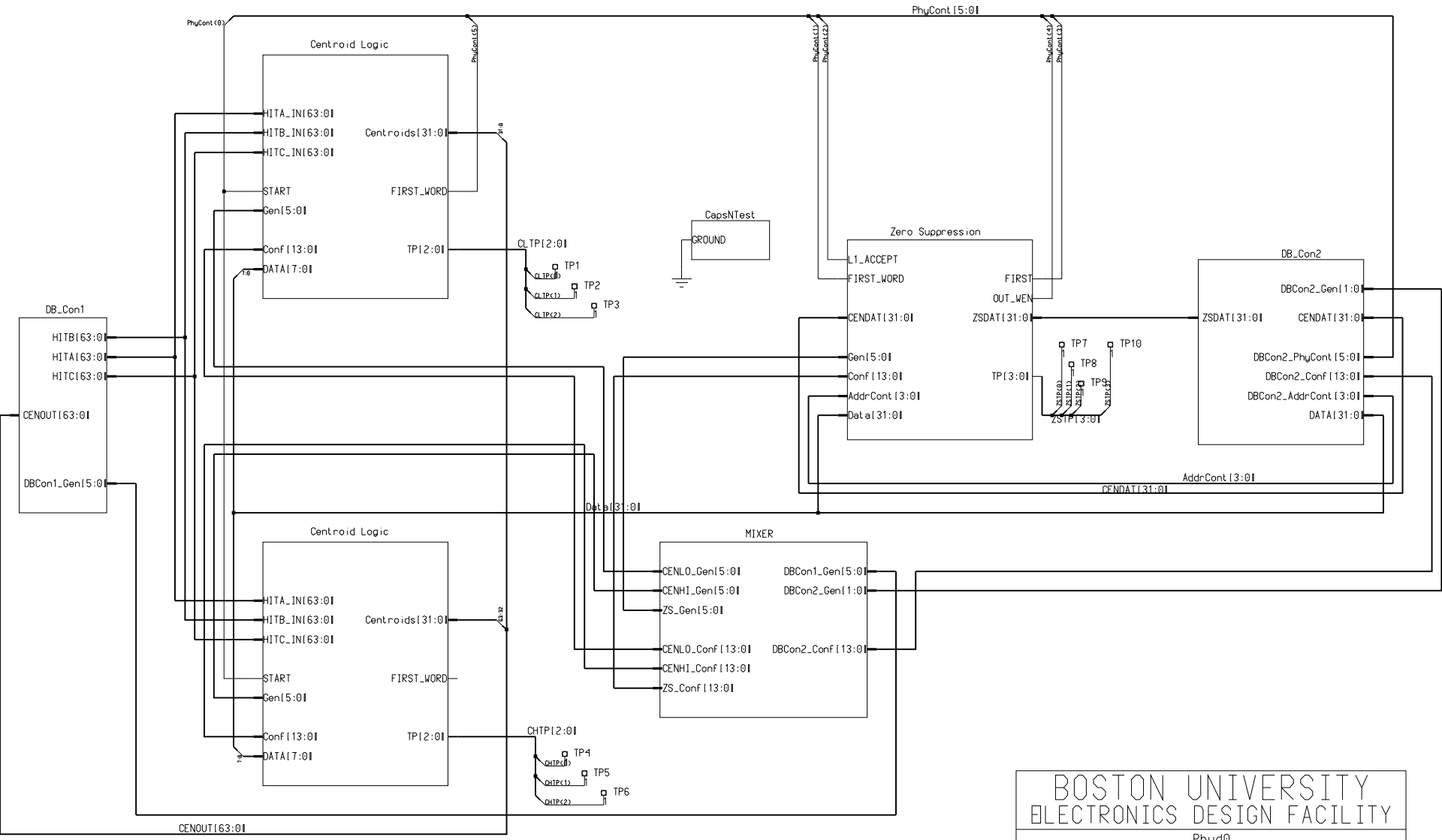
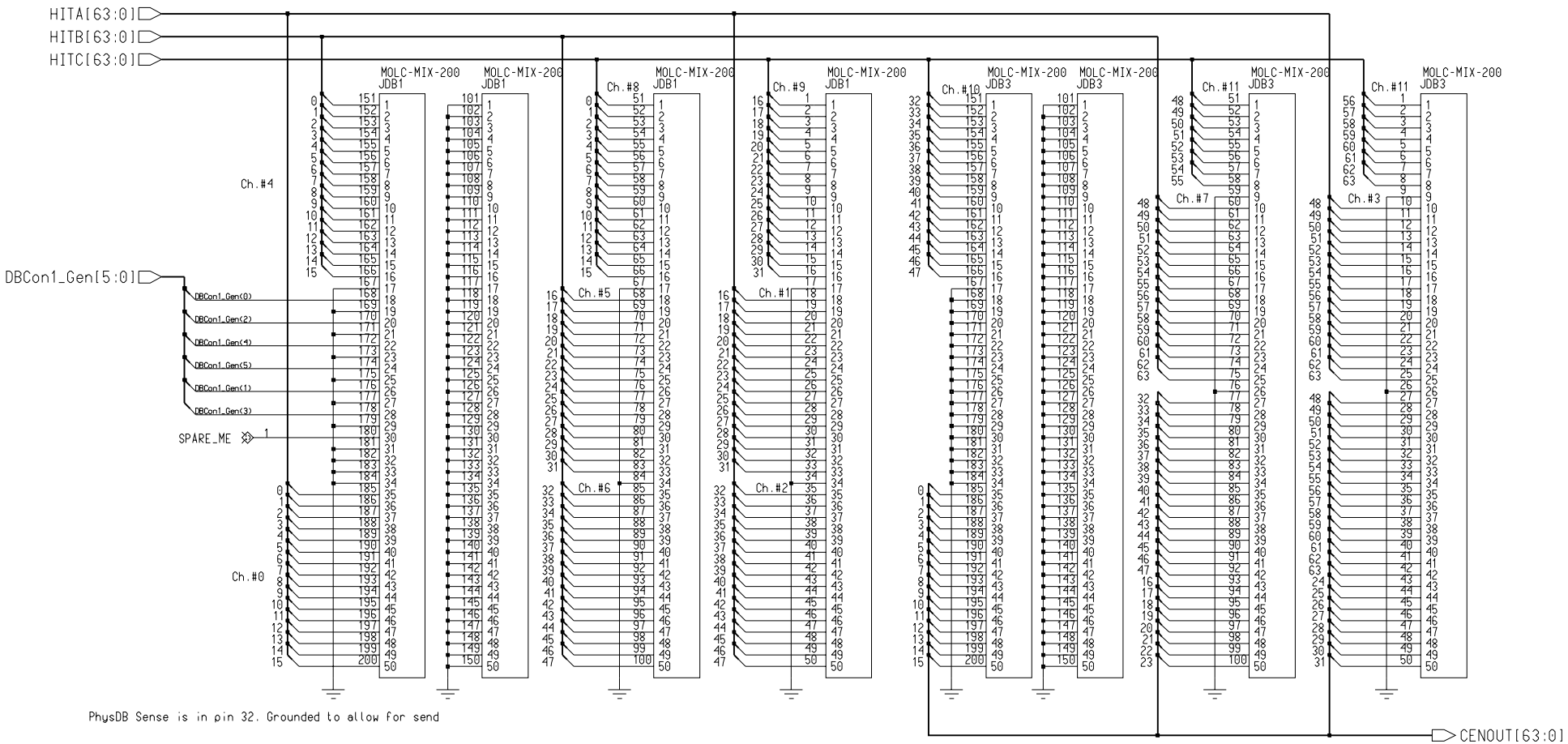


BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

Phyd0
Main Sheet

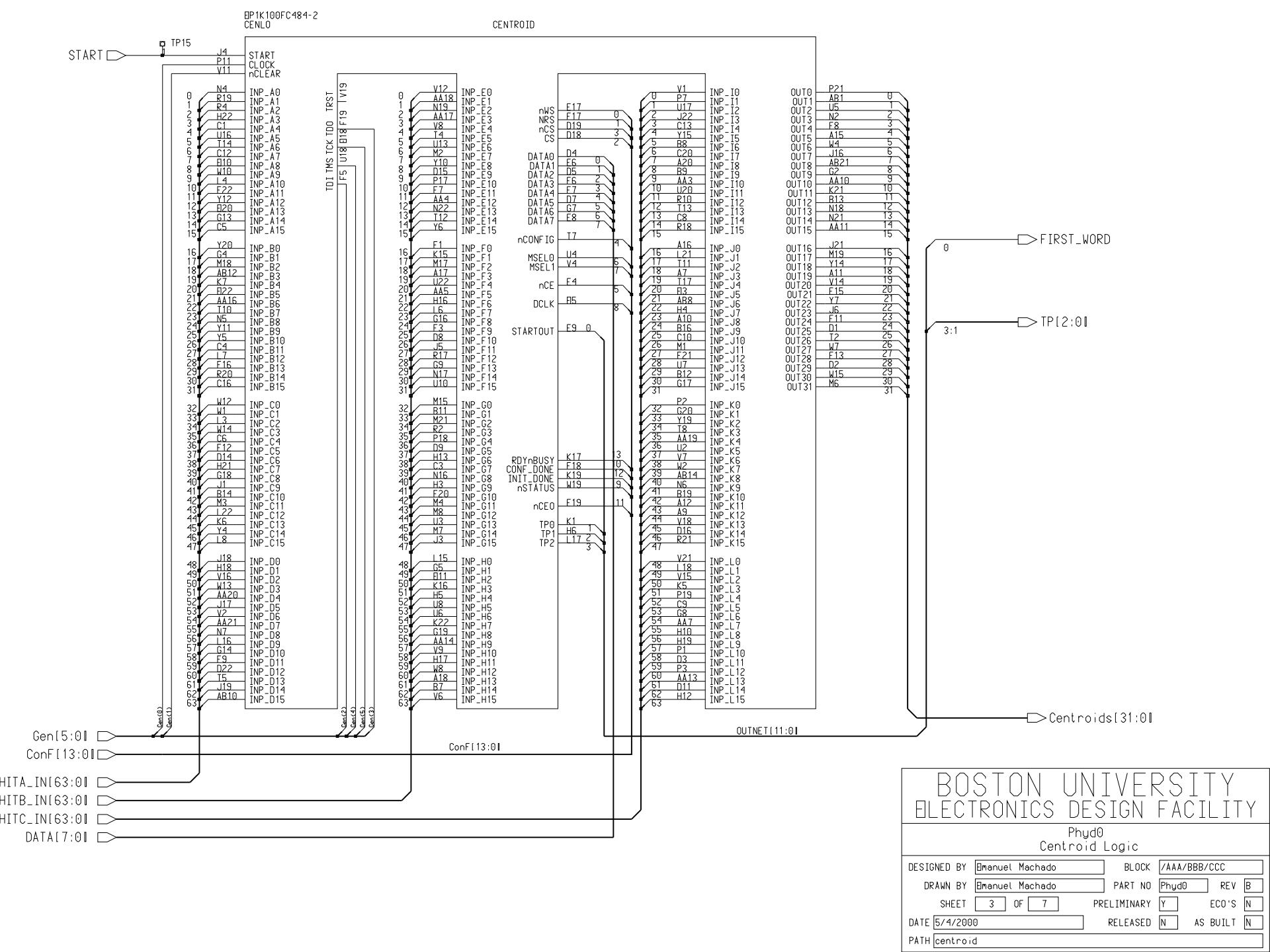
DESIGNED BY	Emanuel Machado	BLOCK			
DRAWN BY	Emanuel Machado	PART NO	Phyd0	REV	B
SHEET	1 OF 7	PRELIMINARY	Y	ECO'S	N
DATE	5/5/2000	RELEASED	N	AS BUILT	N
PATH	/home2/dzero/Phyd0B				



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

PhyD0
Physics Daughterboard Connector 1 and 3

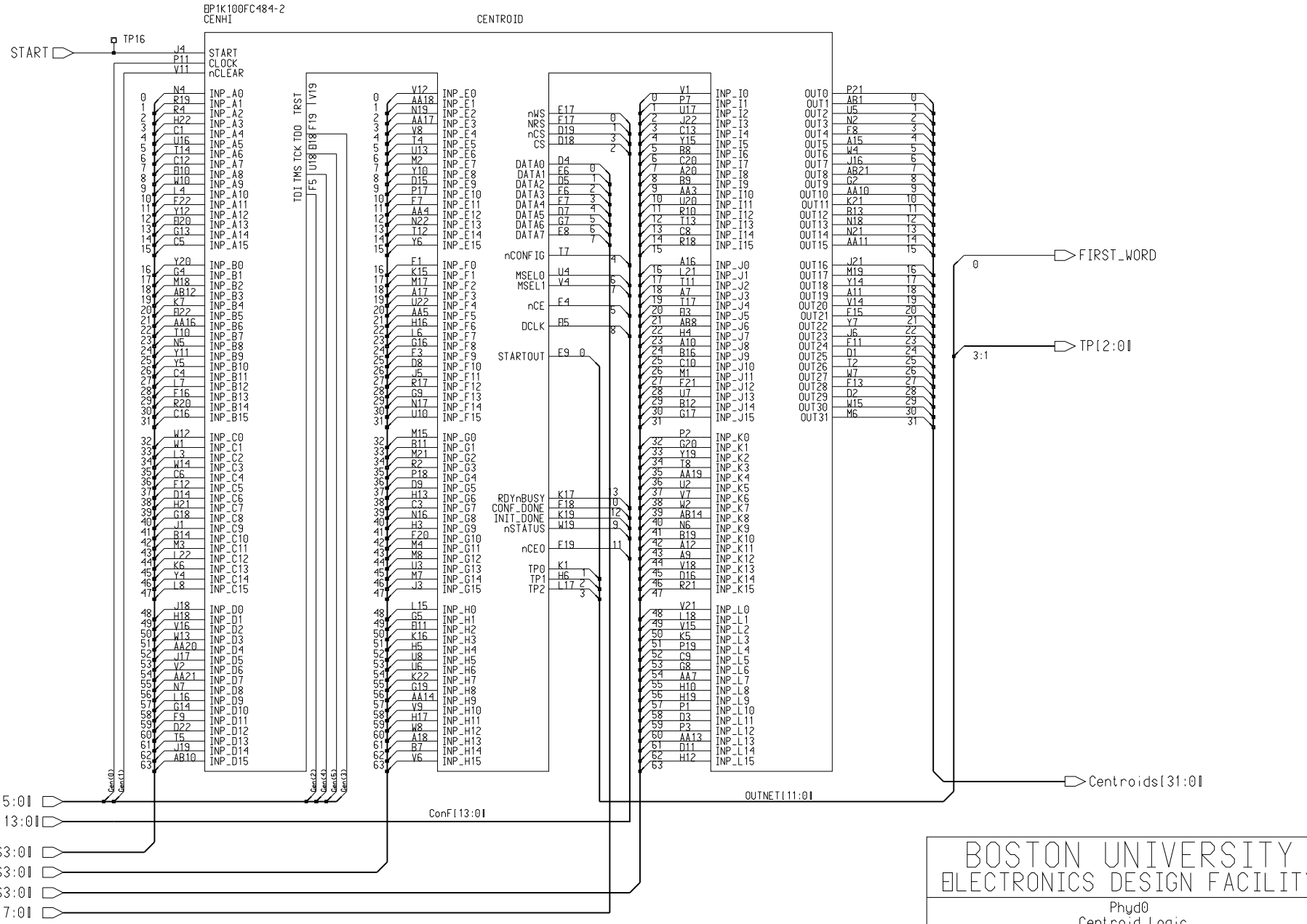
DESIGNED BY	Emanuel Machado		BLOCK	/AAA/BBB/CCC	
DRAWN BY	Emanuel Machado		PART NO	Phyd0	REV B
SHEET	2	OF 7	PRELIMINARY	Y	ECO'S N
DATE	4/5/2000		RELEASED	N	AS BUILT N
PATH	PATH				



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

Phyd0
Centroid Logic

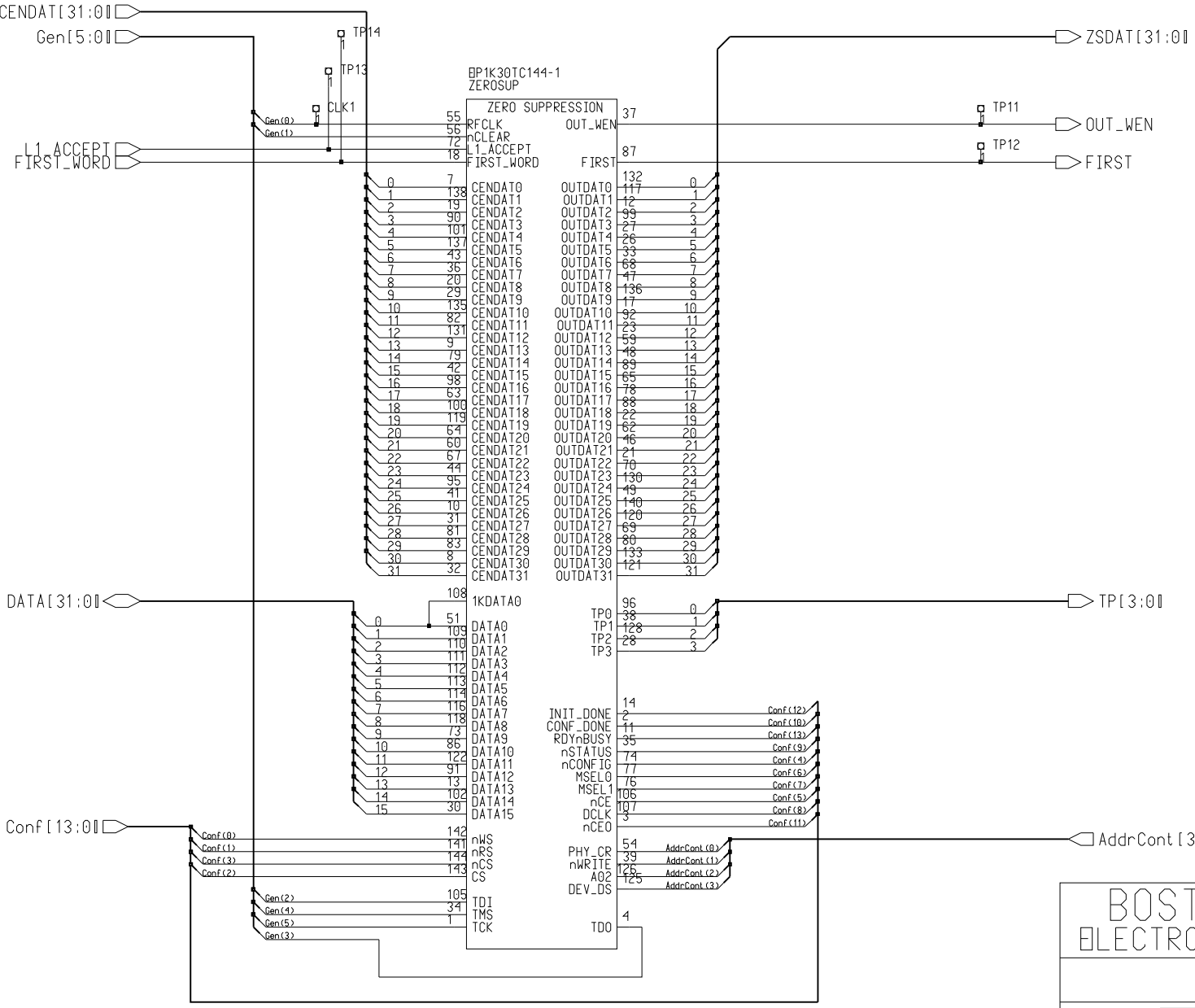
DESIGNED BY	Emanuel Machado	BLOCK	/AAA/BBB/CCC
DRAWN BY	Emanuel Machado	PART NO	Phyd0 REV B
SHEET	3 OF 7	PRELIMINARY	Y ECO'S N
DATE	5/4/2000	RELEASED	N AS BUILT N
PATH	centroid		



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

Phyd0
Centroid Logic

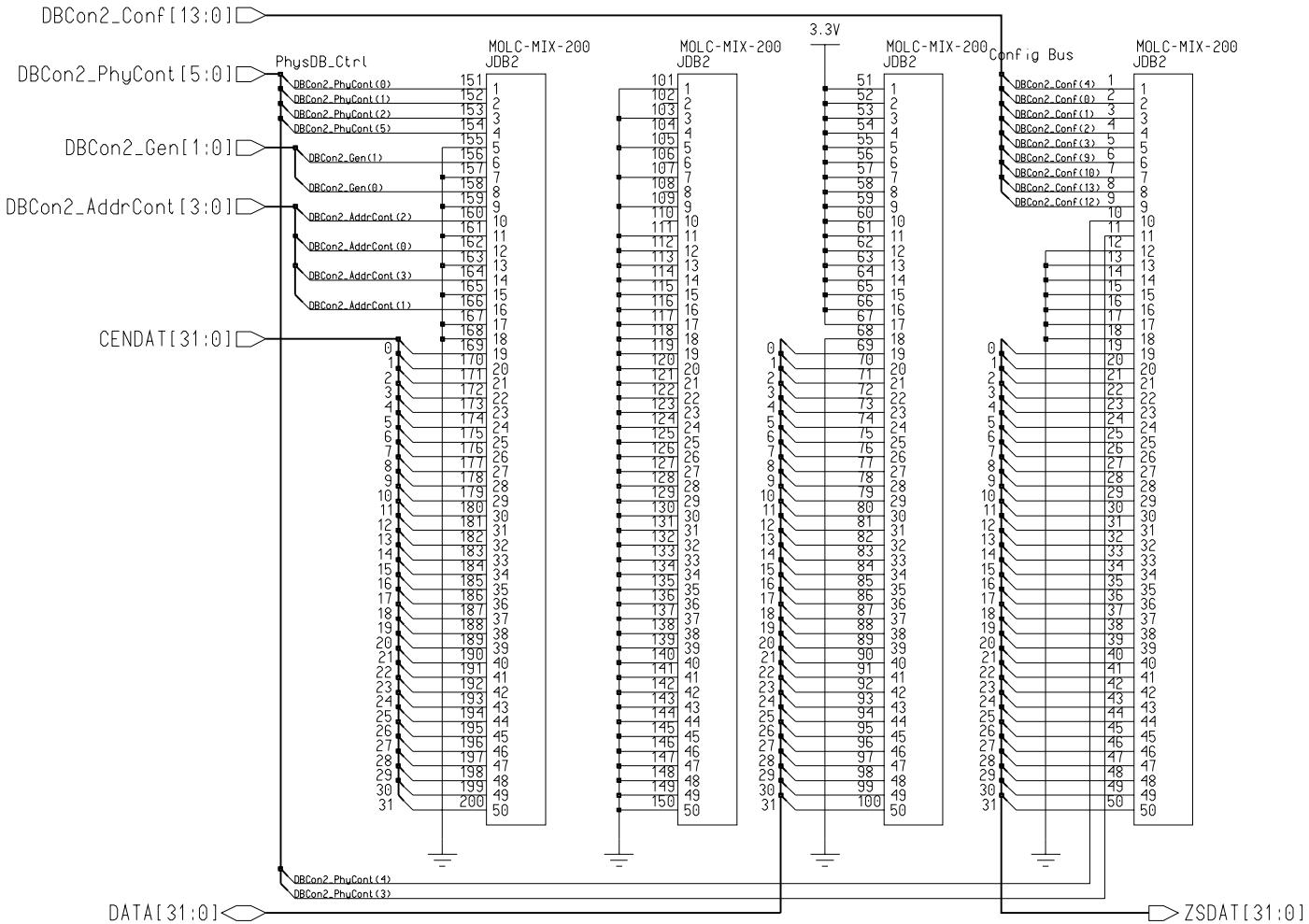
DESIGNED BY	Emanuel Machado	BLOCK	/AAA/BBB/CCC
DRAWN BY	Emanuel Machado	PART NO	Phyd0 REV B
SHEET	3 OF 7	PRELIMINARY	Y ECO'S N
DATE	5/4/2000	RELEASED	N AS BUILT N
PATH	centroid		



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

MCEN
ZERO SUPPRESSION

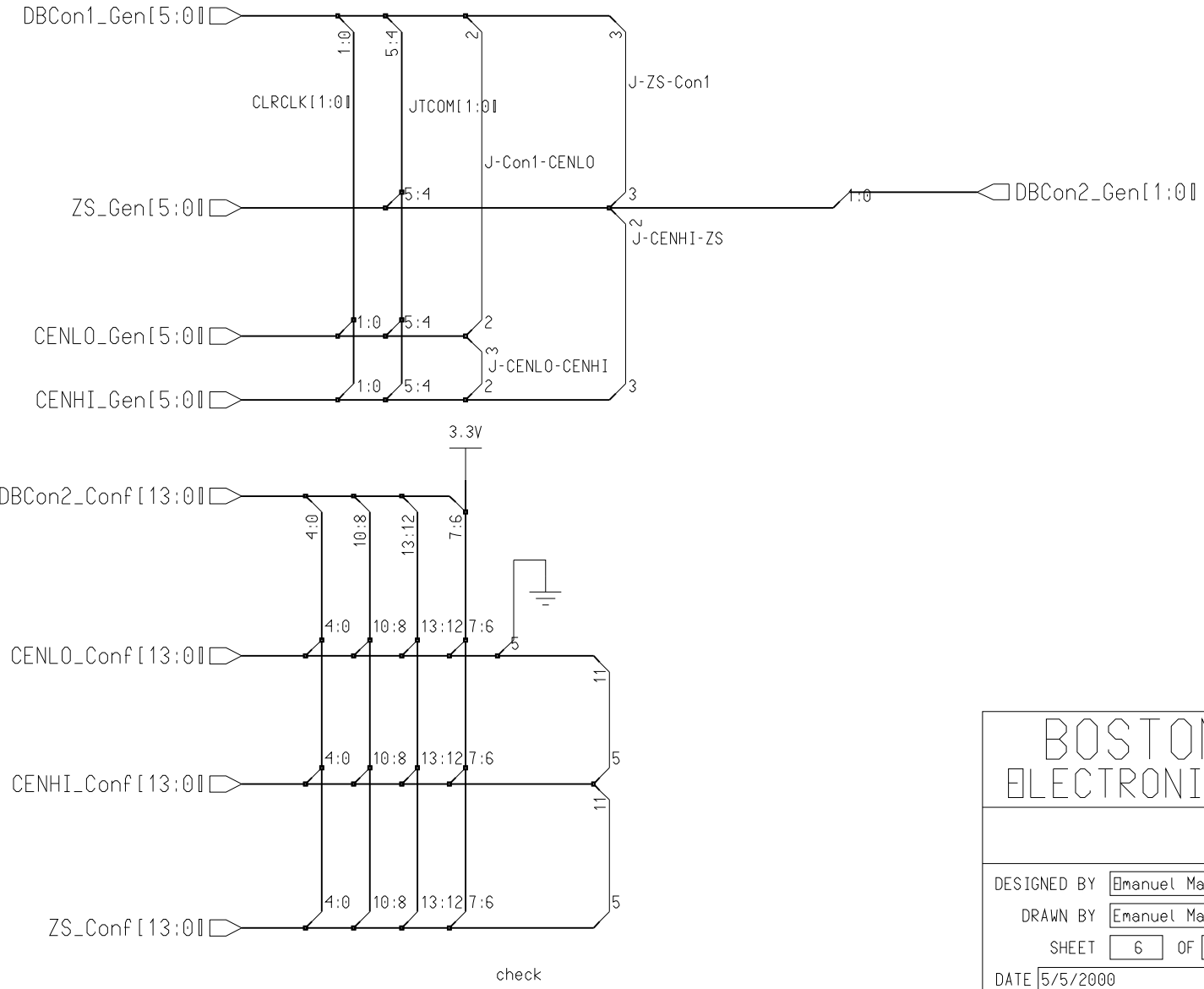
DESIGNED BY	Emanuel Machado	BLOCK	/AAA/BBB/CCC		
DRAWN BY	Emanuel Machado	PART NO	XXX-A	REV	A
SHEET	4 OF 7	PRELIMINARY	Y	ECO'S	N
DATE	5/16/97	RELEASED	N	AS BUILT	N
PATH	zero_suppression				



BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

Phyd0
Physics Daughterboard Connector 2

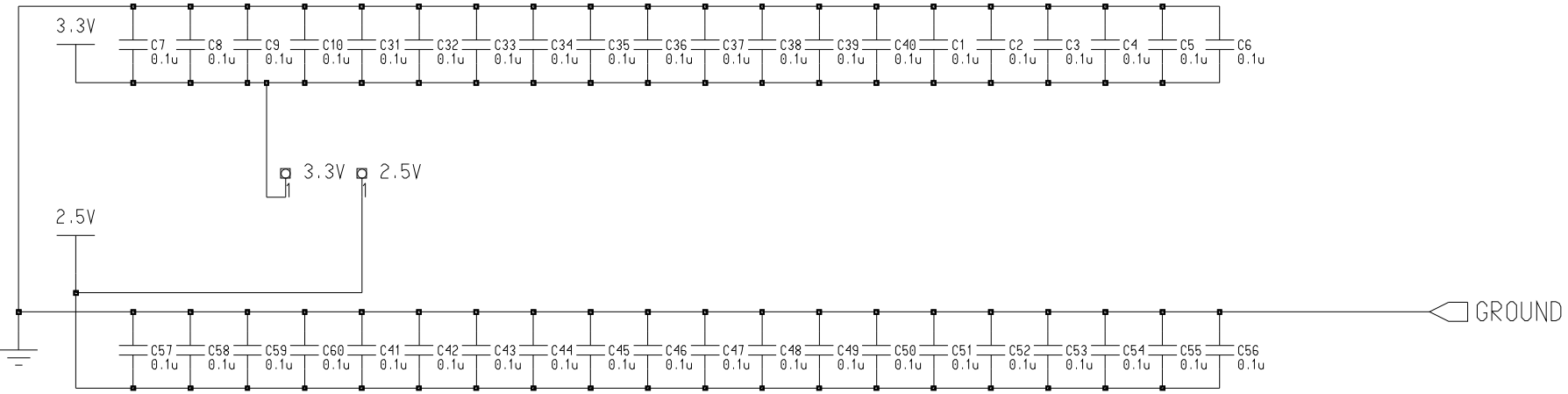
DESIGNED BY	Emanuel Machado	BLOCK	/AAA/BBB/CCC		
DRAWN BY	Emanuel Machado	PART NO	Phyd0	REV	B
SHEET	5 OF 7	PRELIMINARY	Y	ECO'S	N
DATE	5/5/2000	RELEASED	N	AS BUILT	N
PATH	PATH				

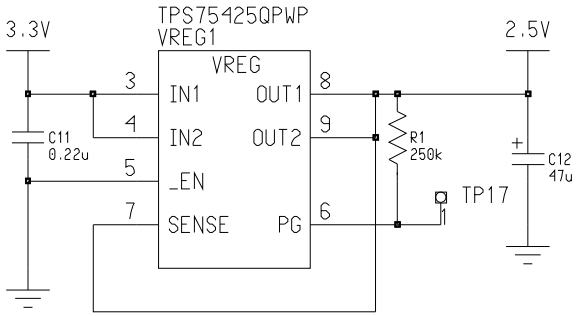


BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

Phyd0
Bus Mixer

DESIGNED BY	Emanuel Machado	BLOCK			
DRAWN BY	Emanuel Machado	PART NO	Phyd0	REV	B
SHEET	6 OF 7	PRELIMINARY	Y	ECO'S	N
DATE	5/5/2000	RELEASED	N	AS BUILT	N
PATH	/home2/dzero/Phyd0B/design_lib/mixer				

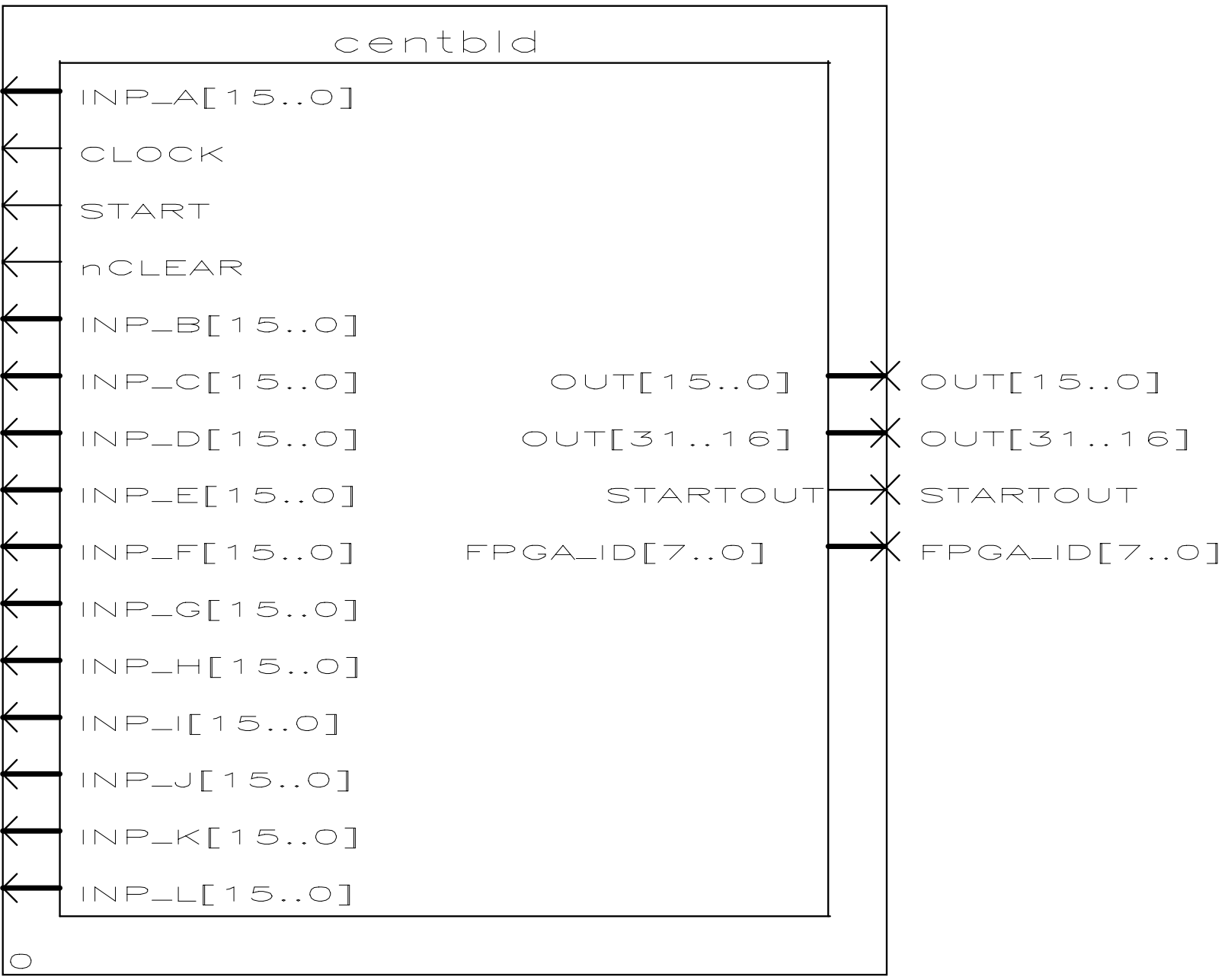




BOSTON UNIVERSITY
ELECTRONICS DESIGN FACILITY

MCEN Physics Board
Capacitors and PowerTest Points

DESIGNED BY	Emanuel Machado	BLOCK	/AAA/BBB/CCC		
DRAWN BY	Emanuel Machado	PART NO	XXX-A	REV	A
SHEET	7 OF 7	PRELIMINARY	Y	ECO'S	N
DATE	4/16/98	RELEASED	N	AS BUILT	N
PATH	PATH				


centbld
INP_A[15..0]
CLOCK
START
nCLEAR
INP_B[15..0]
INP_C[15..0]
INP_D[15..0]
INP_E[15..0]
INP_F[15..0]
INP_G[15..0]
INP_H[15..0]
INP_I[15..0]
INP_J[15..0]
INP_K[15..0]
INP_L[15..0]
OUT[15..0]
OUT[31..16]
STARTOUT
FPGA_ID[7..0]
OUT[15..0]
OUT[31..16]
STARTOUT
FPGA_ID[7..0]
0

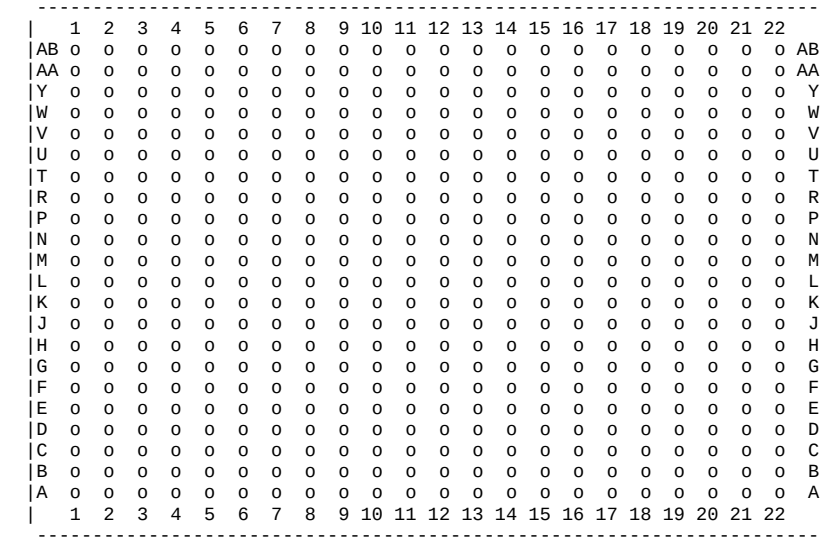
Device-Specific Information:e:\max2work\altera projects\new physics boards\blayer-inner\centbld.rpt
centbld

***** Logic for device 'centbld' compiled without errors.

Device: EP1K100FC484-2

ACEX 1K Configuration Scheme: Passive Parallel Asynchronous

Device Options:
    User-Supplied Start-Up Clock   = OFF
    Auto-Restart Configuration on Frame Error = OFF
    Release Clears Before Tri-States   = OFF
    Enable Chip_Wide Reset   = OFF
    Enable Chip-Wide Output Enable   = OFF
    Enable INIT_DONE Output   = ON
    JTAG User Code   = 7f
    MultiVolt I/O   = ON
    Enable Lock Output   = OFF



EP1K100FC484-2
Bottom View

§
Device-Specific Information:e:\max2work\altera projects\new physics boards\blayer-inner\centbld.rpt
centbld

A1	GND	E10	INP_A8	J19	INP_D14	P6	RESERVED
A2	N.C.	E11	INP_H2	J20	GND	P7	INP_I1
A3	N.C.	E12	GND	J21	OUT16	P8	VCCINT
A4	N.C.	E13	RESERVED	J22	INP_I3	P9	GND
A5	N.C.	E14	RESERVED	K1	FPGA_ID0	P10	VCCINT
A6	VCCIO	E15	OUT21	K2	N.C.	P11	CLOCK
A7	INP_J3	E16	RESERVED	K3	GND	P12	VCC_CKLK
A8	GND	E17	+nWS	K4	RESERVED	P13	VCCIO
A9	INP_K12	E18	#TCK	K5	INP_L3	P14	GND
A10	INP_J8	E19	^nCEO	K6	INP_C13	P15	VCCINT
A11	OUT19	E20	INP_A13	K7	INP_B4	P16	RESERVED
A12	INP_K11	E21	GND	K8	RESERVED	P17	INP_E10
A13	VCCIO	E22	INP_B5	K9	VCCIO	P18	INP_G4
A14	FPGA_ID5	F1	INP_F0	K10	GND	P19	INP_L4
A15	OUT5	F2	N.C.	K11	VCCIO	P20	N.C.
A16	INP_J0	F3	INP_F9	K12	GND	P21	OUT0
A17	INP_F3	F4	FPGA_ID6	K13	GND	P22	N.C.
A18	INP_H13	F5	#TDI	K14	VCCIO	R1	VCCIO
A19	RESERVED	F6	+DATA3	K15	INP_F1	R2	INP_G3
A20	INP_I8	F7	INP_E11	K16	INP_H3	R3	N.C.
A21	RESERVED	F8	OUT4	K17	*RDYnBUSY	R4	INP_A2
A22	GND	F9	INP_D11	K18	RESERVED	R5	RESERVED
B1	GND	F10	GND	K19	@INIT_DONE	R6	RESERVED
B2	GND	F11	OUT24	K20	VCCIO	R7	RESERVED
B3	N.C.	F12	INP_C5	K21	OUT11	R8	GND
B4	N.C.	F13	OUT28	K22	INP_H7	R9	VCCIO
B5	VCCIO	F14	RESERVED	L1	RESERVED	R10	INP_I12
B6	RESERVED	F15	RESERVED	L2	N.C.	R11	RESERVED
B7	INP_H14	F16	INP_B13	L3	INP_C2	R12	GND
B8	INP_I6	F17	+nRS	L4	INP_A10	R13	RESERVED
B9	INP_I9	F18	^CONF_DONE	L5	RESERVED	R14	VCCINT

V15	INP_L2	W19	^nSTATUS
V16	INP_D2	W20	GND
V17	RESERVED	W21	VCCINT
V18	INP_K13	W22	N.C.
V19	#TRST	Y1	GND
V20	RESERVED		
V21	INP_L0		
V22	VCCIO		
W1	INP_C1		
W2	INP_K7		
W3	RESERVED		
W4	OUT6		
W5	RESERVED		
W6	RESERVED		
W7	OUT27		
W8	INP_H12		
W9	RESERVED		
W10	INP_A9		
W11	GND_CKLK		
W12	INP_C0		
W13	INP_D3		
W14	INP_C3		
W15	OUT30		
W16	RESERVED		
W17	RESERVED		
W18	RESERVED		
W19	^nSTATUS		
W20	GND		
W21	VCCINT		
W22	N.C.		
Y1	GND		

B10	N.C.	F19	#TDO	L6	INP_F7	R15	GND	Y2	GND
B11	INP_G1	F20	INP_G10	L7	INP_B12	R16	RESERVED	Y3	GND
B12	INP_J14	F21	INP_J12	L8	INP_C15	R17	INP_F12	Y4	INP_C14
B13	OUT12	F22	INP_A11	L9	VCCINT	R18	INP_I15	Y5	INP_B10
B14	INP_C10	G1	VCCIO	L10	VCCINT	R19	INP_A1	Y6	INP_E15
B15	RESERVED	G2	OUT9	L11	GND	R20	INP_B14	Y7	OUT22
B16	INP_J9	G3	GND	L12	GND	R21	INP_K15	Y8	VCCINT
B17	GND	G4	INP_B1	L13	VCCINT	R22	GND	Y9	RESERVED
B18	RESERVED	G5	INP_H1	L14	VCCIO	T1	GND	Y10	INP_E8
B19	INP_K10	G6	RESERVED	L15	INP_H0	T2	OUT26	Y11	INP_B9
B20	RESERVED	G7	+DATA6	L16	INP_D9	T3	VCCIO	Y12	INP_A12
B21	GND	G8	INP_L6	L17	FPGA_ID2	T4	INP_E5	Y13	RESERVED
B22	GND	G9	INP_F13	L18	INP_L1	T5	INP_D13	Y14	OUT18
C1	INP_A4	G10	RESERVED	L19	RESERVED	T6	RESERVED	Y15	INP_I5
C2	GND	G11	RESERVED	L20	RESERVED	T7	^nCONFIG	Y16	N.C.
C3	INP_G7	G12	RESERVED	L21	INP_J1	T8	INP_K3	Y17	RESERVED
C4	INP_B11	G13	INP_A14	L22	INP_C12	T9	RESERVED	Y18	RESERVED
C5	INP_A15	G14	INP_D10	M1	INP_J11	T10	INP_B7	Y19	INP_K2
C6	INP_C4	G15	VCCIO	M2	INP_E7	T11	INP_J2	Y20	INP_B0
C7	RESERVED	G16	INP_F8	M3	INP_C11	T12	INP_E14	Y21	GND
C8	INP_I14	G17	INP_J15	M4	INP_G11	T13	INP_I13	Y22	GND
C9	INP_L5	G18	INP_C8	M5	RESERVED	T14	INP_A6	AA1	GND
C10	INP_J10	G19	INP_H8	M6	OUT31	T15	VCCIO	AA2	RESERVED
C11	VCCINT	G20	INP_K1	M7	INP_G14	T16	RESERVED	AA3	INP_I10
C12	INP_A7	G21	GND	M8	INP_G12	T17	INP_J4	AA4	INP_E12
C13	INP_I4	G22	RESERVED	M9	VCCIO	T18	RESERVED	AA5	INP_F5
C14	RESERVED	H1	RESERVED	M10	VCCINT	T19	RESERVED	AA6	GND
C15	VCCINT	H2	GND	M11	GND	T20	N.C.	AA7	INP_L7
C16	INP_B15	H3	INP_G9	M12	GND	T21	N.C.	AA8	RESERVED
C17	N.C.	H4	INP_J7	M13	VCCINT	T22	VCCIO	AA9	RESERVED
C18	RESERVED	H5	INP_H4	M14	VCCINT	U1	N.C.	AA10	OUT10
C19	RESERVED	H6	FPGA_ID1	M15	INP_G0	U2	INP_K5	AA11	OUT15
C20	INP_I7	H7	RESERVED	M16	RESERVED	U3	INP_G13	AA12	VCCINT
C21	GND	H8	GND	M17	INP_F2	U4	^MSEL0	AA13	INP_L13
C22	RESERVED	H9	VCCIO	M18	INP_B2	U5	OUT2	AA14	INP_H9
D1	OUT25	H10	INP_L8	M19	OUT17	U6	INP_H6	AA15	N.C.
D2	OUT29	H11	GND	M20	GND	U7	INP_J13	AA16	INP_B6
D3	INP_L11	H12	INP_L15	M21	INP_G2	U8	INP_H5	AA17	INP_E3
D4	^DATA0	H13	INP_G6	M22	RESERVED	U9	RESERVED	AA18	INP_E1
D5	+DATA2	H14	VCCINT	N1	N.C.	U10	INP_F15	AA19	INP_K4
D6	GND	H15	GND	N2	OUT3	U11	RESERVED	AA20	INP_D4
D7	+DATA5	H16	INP_F6	N3	VCCIO	U12	RESERVED	AA21	INP_D7
D8	INP_F10	H17	INP_H11	N4	INP_A0	U13	INP_E6	AA22	GND
D9	INP_G5	H18	INP_D1	N5	INP_B8	U14	FPGA_ID4	AB1	OUT1
D10	RESERVED	H19	INP_L9	N6	INP_K9	U15	RESERVED	AB2	RESERVED
D11	INP_L14	H20	VCCIO	N7	INP_D8	U16	INP_A5	AB3	N.C.
D12	GND	H21	INP_C7	N8	GND	U17	INP_I2	AB4	N.C.
D13	RESERVED	H22	INP_A3	N9	VCCIO	U18	#TMS	AB5	N.C.
D14	INP_C6	J1	INP_C9	N10	GND	U19	RESERVED	AB6	FPGA_ID7
D15	INP_E9	J2	N.C.	N11	VCCIO	U20	INP_I11	AB7	N.C.
D16	INP_K14	J3	INP_G15	N12	VCCINT	U21	RESERVED	AB8	INP_J6
D17	GND	J4	START	N13	GND	U22	INP_F4	AB9	RESERVED
D18	+CS	J5	INP_F11	N14	VCCIO	V1	INP_I0	AB10	INP_D15
D19	+nCS	J6	OUT23	N15	RESERVED	V2	INP_D6	AB11	GND
D20	RESERVED	J7	RESERVED	N16	INP_G8	V3	GND	AB12	INP_B3
D21	FPGA_ID3	J8	VCCINT	N17	INP_F14	V4	^MSEL1	AB13	VCCIO
D22	INP_D12	J9	GND	N18	OUT13	V5	VCCINT	AB14	INP_K8
E1	VCCIO	J10	VCCINT	N19	INP_E2	V6	INP_H15	AB15	N.C.
E2	RESERVED	J11	VCCIO	N20	VCCIO	V7	INP_K6	AB16	GND
E3	INP_J5	J12	VCCINT	N21	OUT14	V8	INP_E4	AB17	N.C.
E4	^nCE	J13	VCCIO	N22	INP_E13	V9	INP_H10	AB18	N.C.
E5	^DCLK	J14	GND	P1	INP_L10	V10	RESERVED	AB19	N.C.
E6	+DATA1	J15	VCCINT	P2	INP_K0	V11	nCLEAR	AB20	N.C.
E7	+DATA4	J16	OUT7	P3	INP_L12	V12	INP_E0	AB21	OUT8
E8	+DATA7	J17	INP_D5	P4	GND	V13	RESERVED	AB22	RESERVED
E9	STARTOUT	J18	INP_D0	P5	RESERVED	V14	OUT20		

N.C. = No Connect. This pin has no internal connection to the device.
VCCINT = Dedicated power pin, which MUST be connected to VCC (2.5 volts).
VCCIO = Dedicated power pin, which MUST be connected to VCC (2.5 volts).
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.

^ = Dedicated configuration pin.
+ = Reserved configuration pin, which is tri-stated during user mode.
* = Reserved configuration pin, which drives out in user mode.
PDn = Power Down pin.
@ = Special-purpose pin.
# = JTAG Boundary-Scan Testing/In-System Programming or Configuration Pin. The JTAG inputs TMS and TDI should be tied to VCC and TCK should be tied to GND when not in use.
& = JTAG pin used for I/O. When used as user I/O, JTAG pins must be kept stable before and during configuration. JTAG pin stability prevents accidental loading of JTAG instructions.
$ = Pin has PCI I/O option enabled. Pin is neither ’5.0 V’- nor ’3.3 V’-tolerant.

N.C. = No Connect. This pin has no internal connection to the device.
VCCINT = Dedicated power pin, which MUST be connected to VCC (2.5 volts).
VCCIO = Dedicated power pin, which MUST be connected to VCC (2.5 volts).
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.

CHIP "centbld" ASSIGNED TO AN EP1K100FC484-2

GND	: AA1
RESERVED	: AA2
INP_I10	: AA3
INP_E12	: AA4
INP_F5	: AA5
GND	: AA6
INP_L7	: AA7
RESERVED	: AA8
RESERVED	: AA9
OUT10	: AA10
OUT15	: AA11
VCCINT	: AA12
INP_L13	: AA13
INP_H9	: AA14
N.C.	: AA15
INP_B6	: AA16
INP_E3	: AA17
INP_E1	: AA18
INP_K4	: AA19
INP_D4	: AA20
INP_D7	: AA21
GND	: AA22
OUT1	: AB1
RESERVED	: AB2
N.C.	: AB3
N.C.	: AB4
N.C.	: AB5
FPGA_ID7	: AB6
N.C.	: AB7
INP_J6	: AB8
RESERVED	: AB9
INP_D15	: AB10
GND	: AB11
INP_B3	: AB12
VCCIO	: AB13
INP_K8	: AB14
N.C.	: AB15
GND	: AB16
N.C.	: AB17
N.C.	: AB18
N.C.	: AB19
N.C.	: AB20
OUT8	: AB21
RESERVED	: AB22
GND	: A1
N.C.	: A2
N.C.	: A3
N.C.	: A4
N.C.	: A5
VCCIO	: A6
INP_J3	: A7
GND	: A8
INP_K12	: A9
INP_J8	: A10
OUT19	: A11
INP_K11	: A12
VCCIO	: A13
FPGA_ID5	: A14
OUT5	: A15
INP_J0	: A16
INP_F3	: A17
INP_H13	: A18
RESERVED	: A19

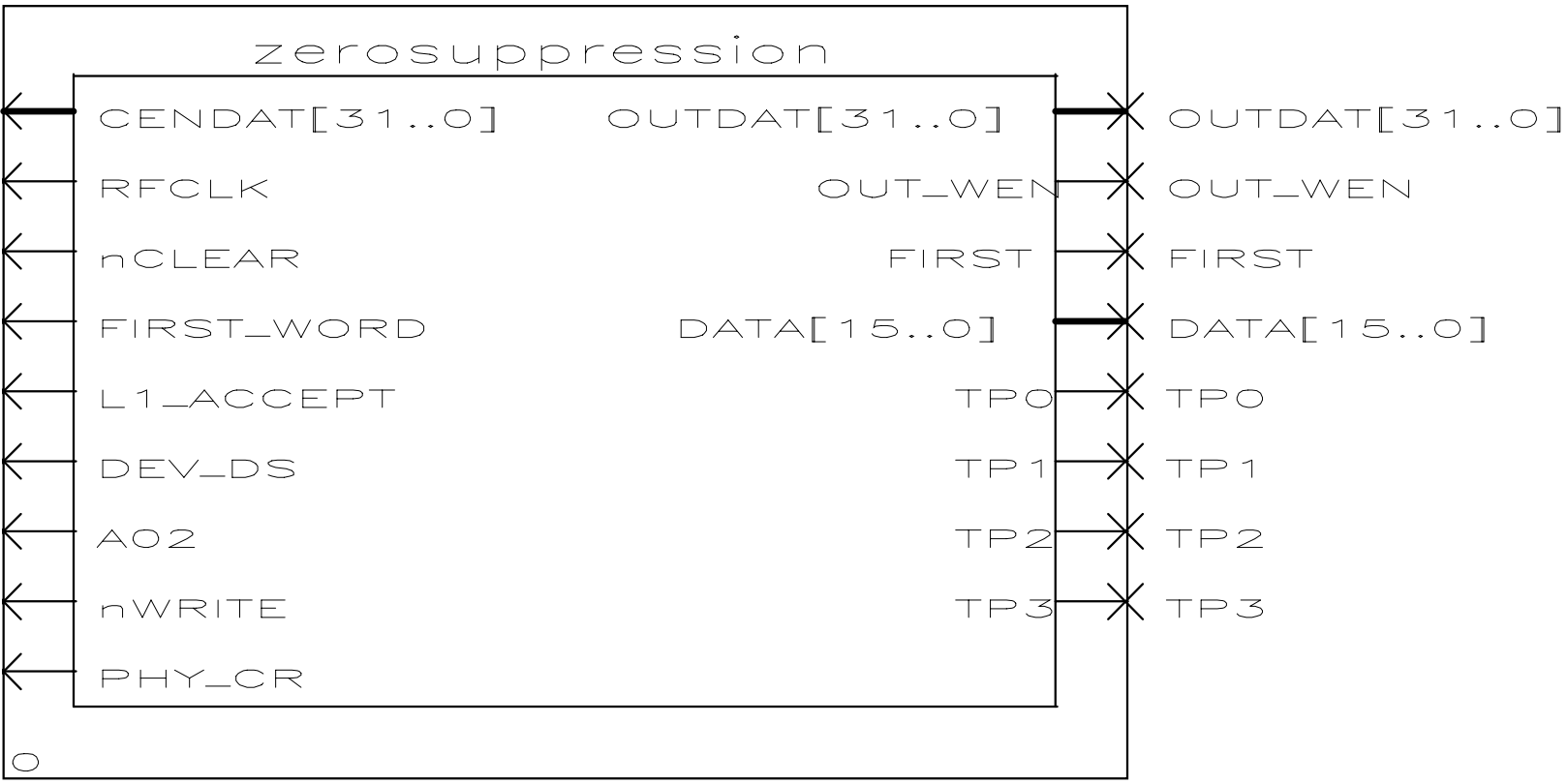
INP_I8 : A20
RESERVED : A21
GND : A22
GND : B1
GND : B2
N.C. : B3
N.C. : B4
VCCIO : B5
RESERVED : B6
INP_H14 : B7
INP_I6 : B8
INP_I9 : B9
N.C. : B10
INP_G1 : B11
INP_J14 : B12
OUT12 : B13
INP_C10 : B14
RESERVED : B15
INP_J9 : B16
GND : B17
RESERVED : B18
INP_K10 : B19
RESERVED : B20
GND : B21
GND : B22
INP_A4 : C1
GND : C2
INP_G7 : C3
INP_B11 : C4
INP_A15 : C5
INP_C4 : C6
RESERVED : C7
INP_I14 : C8
INP_L5 : C9
INP_J10 : C10
VCCINT : C11
INP_A7 : C12
INP_I4 : C13
RESERVED : C14
VCCINT : C15
INP_B15 : C16
N.C. : C17
RESERVED : C18
RESERVED : C19
INP_I7 : C20
GND : C21
RESERVED : C22
OUT25 : D1
OUT29 : D2
INP_L11 : D3
DATA0 : D4
DATA2 : D5
GND : D6
DATA5 : D7
INP_F10 : D8
INP_G5 : D9
RESERVED : D10
INP_L14 : D11
GND : D12
RESERVED : D13
INP_C6 : D14
INP_E9 : D15
INP_K14 : D16
GND : D17
CS : D18
nCS : D19
RESERVED : D20
FPGA_ID3 : D21
INP_D12 : D22
VCCIO : E1
RESERVED : E2
INP_J5 : E3
nCE : E4
DCLK : E5
DATA1 : E6
DATA4 : E7
DATA7 : E8
STARTOUT : E9
INP_A8 : E10
INP_H2 : E11
GND : E12
RESERVED : E13
RESERVED : E14
OUT21 : E15
RESERVED : E16
nWS : E17
TCK : E18
nCEO : E19
INP_A13 : E20
GND : E21
INP_B5 : E22
INP_F0 : F1
N.C. : F2
INP_F9 : F3

FPGA_ID6 : F4
TDI : F5
DATA3 : F6
INP_E11 : F7
OUT4 : F8
INP_D11 : F9
GND : F10
OUT24 : F11
INP_C5 : F12
OUT28 : F13
RESERVED : F14
RESERVED : F15
INP_B13 : F16
nRS : F17
CONF_DONE : F18
TDO : F19
INP_G10 : F20
INP_J12 : F21
INP_A11 : F22
VCCIO : G1
OUT9 : G2
GND : G3
INP_B1 : G4
INP_H1 : G5
RESERVED : G6
DATA6 : G7
INP_L6 : G8
INP_F13 : G9
RESERVED : G10
RESERVED : G11
RESERVED : G12
INP_A14 : G13
INP_D10 : G14
VCCIO : G15
INP_F8 : G16
INP_J15 : G17
INP_C8 : G18
INP_H8 : G19
INP_K1 : G20
GND : G21
RESERVED : G22
RESERVED : H1
GND : H2
INP_G9 : H3
INP_J7 : H4
INP_H4 : H5
FPGA_ID1 : H6
RESERVED : H7
GND : H8
VCCIO : H9
INP_L8 : H10
GND : H11
INP_L15 : H12
INP_G6 : H13
VCCINT : H14
GND : H15
INP_F6 : H16
INP_H11 : H17
INP_D1 : H18
INP_L9 : H19
VCCIO : H20
INP_C7 : H21
INP_A3 : H22
INP_C9 : J1
N.C. : J2
INP_G15 : J3
START : J4
INP_F11 : J5
OUT23 : J6
RESERVED : J7
VCCINT : J8
GND : J9
VCCINT : J10
VCCIO : J11
VCCINT : J12
VCCIO : J13
GND : J14
VCCINT : J15
OUT7 : J16
INP_D5 : J17
INP_D0 : J18
INP_D14 : J19
GND : J20
OUT16 : J21
INP_I3 : J22
FPGA_ID0 : K1
N.C. : K2
GND : K3
RESERVED : K4
INP_L3 : K5
INP_C13 : K6
INP_B4 : K7
RESERVED : K8
VCCIO : K9

GND : K10
VCCIO : K11
GND : K12
GND : K13
VCCIO : K14
INP_F1 : K15
INP_H3 : K16
RDYnBUSY : K17
RESERVED : K18
INIT_DONE : K19
VCCIO : K20
OUT11 : K21
INP_H7 : K22
RESERVED : L1
N.C. : L2
INP_C2 : L3
INP_A10 : L4
RESERVED : L5
INP_F7 : L6
INP_B12 : L7
INP_C15 : L8
VCCINT : L9
VCCINT : L10
GND : L11
GND : L12
VCCINT : L13
VCCIO : L14
INP_H0 : L15
INP_D9 : L16
FPGA_ID2 : L17
INP_L1 : L18
RESERVED : L19
RESERVED : L20
INP_J1 : L21
INP_C12 : L22
INP_J11 : M1
INP_E7 : M2
INP_C11 : M3
INP_G11 : M4
RESERVED : M5
OUT31 : M6
INP_G14 : M7
INP_G12 : M8
VCCIO : M9
VCCINT : M10
GND : M11
GND : M12
VCCINT : M13
VCCINT : M14
INP_G0 : M15
RESERVED : M16
INP_F2 : M17
INP_B2 : M18
OUT17 : M19
GND : M20
INP_G2 : M21
RESERVED : M22
N.C. : N1
OUT3 : N2
VCCIO : N3
INP_A0 : N4
INP_B8 : N5
INP_K9 : N6
INP_D8 : N7
GND : N8
VCCIO : N9
GND : N10
VCCIO : N11
VCCINT : N12
GND : N13
VCCIO : N14
RESERVED : N15
INP_G8 : N16
INP_F14 : N17
OUT13 : N18
INP_E2 : N19
VCCIO : N20
OUT14 : N21
INP_E13 : N22
INP_L10 : P1
INP_K0 : P2
INP_L12 : P3
GND : P4
RESERVED : P5
RESERVED : P6
INP_I1 : P7
VCCINT : P8
GND : P9
VCCINT : P10
CLOCK : P11
VCC_CKLK : P12
VCCIO : P13
GND : P14
VCCINT : P15

RESERVED : P16
INP_E10 : P17
INP_G4 : P18
INP_L4 : P19
N.C. : P20
OUT0 : P21
N.C. : P22
VCCIO : R1
INP_G3 : R2
N.C. : R3
INP_A2 : R4
RESERVED : R5
RESERVED : R6
RESERVED : R7
GND : R8
VCCIO : R9
INP_I12 : R10
RESERVED : R11
GND : R12
RESERVED : R13
VCCINT : R14
GND : R15
RESERVED : R16
INP_F12 : R17
INP_I15 : R18
INP_A1 : R19
INP_B14 : R20
INP_K15 : R21
GND : R22
GND : T1
OUT26 : T2
VCCIO : T3
INP_E5 : T4
INP_D13 : T5
RESERVED : T6
nCONFIG : T7
INP_K3 : T8
RESERVED : T9
INP_B7 : T10
INP_J2 : T11
INP_E14 : T12
INP_I13 : T13
INP_A6 : T14
VCCIO : T15
RESERVED : T16
INP_J4 : T17
RESERVED : T18
RESERVED : T19
N.C. : T20
N.C. : T21
VCCIO : T22
N.C. : U1
INP_K5 : U2
INP_G13 : U3
MSEL0 : U4
OUT2 : U5
INP_H6 : U6
INP_J13 : U7
INP_H5 : U8
RESERVED : U9
INP_F15 : U10
RESERVED : U11
RESERVED : U12
INP_E6 : U13
FPGA_ID4 : U14
RESERVED : U15
INP_A5 : U16
INP_I2 : U17
TMS : U18
RESERVED : U19
INP_I11 : U20
RESERVED : U21
INP_F4 : U22
INP_I0 : V1
INP_D6 : V2
GND : V3
MSEL1 : V4
VCCINT : V5
INP_H15 : V6
INP_K6 : V7
INP_E4 : V8
INP_H10 : V9
RESERVED : V10
nCLEAR : V11
INP_E0 : V12
RESERVED : V13
OUT20 : V14
INP_L2 : V15
INP_D2 : V16
RESERVED : V17
INP_K13 : V18
TRST : V19
RESERVED : V20
INP_L0 : V21

VCCIO : V22
INP_C1 : W1
INP_K7 : W2
RESERVED : W3
OUT6 : W4
RESERVED : W5
RESERVED : W6
OUT27 : W7
INP_H12 : W8
RESERVED : W9
INP_A9 : W10
GND_CKLK : W11
INP_C0 : W12
INP_D3 : W13
INP_C3 : W14
OUT30 : W15
RESERVED : W16
RESERVED : W17
RESERVED : W18
nSTATUS : W19
GND : W20
VCCINT : W21
N.C. : W22
GND : Y1
GND : Y2
GND : Y3
INP_C14 : Y4
INP_B10 : Y5
INP_E15 : Y6
OUT22 : Y7
VCCINT : Y8
RESERVED : Y9
INP_E8 : Y10
INP_B9 : Y11
INP_A12 : Y12
RESERVED : Y13
OUT18 : Y14
INP_I5 : Y15
N.C. : Y16
RESERVED : Y17
RESERVED : Y18
INP_K2 : Y19
INP_B0 : Y20
GND : Y21
GND : Y22


zerosuppression
CENDAT[31..0]
RFCLK
nCLEAR
FIRST_WORD
L1_ACCEPT
DEV_DS
A02
nWRITE
PHY_CR
OUTDAT[31..0]
OUT_WEN
FIRST
DATA[15..0]
TP0
TP1
TP2
TP3
OUTDAT[31..0]
OUT_WEN
FIRST
DATA[15..0]
TP0
TP1
TP2
TP3

```
                        O         C   O   C O                 O O C
                        U   C C O E   U O E U                 U U E   O
                        T   E E U N   T U N T     V   D     D T T N   U
                        D   N N T D V D T D D     C   E     A D D D D T D V D D D D D D
                +   + + A   D D D A C A D A A     C   V     T A A A A D A C A A A A A A
                n + n n T G A A A T C T A T T G T I A _ G G A T T T T A T C T T T T T T
                C C W R 2 N T T T 1 I 3 T 1 2 N P N 0 D N N 1 3 2 1 A T A I A A A A A A
                S S S S 6 D 1 5 9 0 O 0 0 2 4 D 2 T 2 S D D 1 1 7 9 8 1 7 O 6 5 4 3 2 1
              --------------------------------------------------------------------------_
             / 144 142 140 138 136 134 132 130 128 126 124 122 120 118 116 114 112 110   |_
            /    143 141 139 137 135 133 131 129 127 125 123 121 119 117 115 113 111 109    |
      #TCK |  1                                                                        108 | ^DATA0
^CONF_DONE |  2                                                                        107 | ^DCLK
     ^nCEO |  3                                                                        106 | ^nCE
      #TDO |  4                                                                        105 | #TDI
     VCCIO |  5                                                                        104 | GND
       GND |  6                                                                        103 | VCCINT
   CENDAT0 |  7                                                                        102 | DATA14
  CENDAT30 |  8                                                                        101 | CENDAT4
  CENDAT13 |  9                                                                        100 | CENDAT18
  CENDAT26 | 10                                                                         99 | OUTDAT3
 *RDYnBUSY | 11                                                                         98 | CENDAT16
   OUTDAT2 | 12                                                                         97 | RESERVED
    DATA13 | 13                                                                         96 | TP0
@INIT_DONE | 14                                                                         95 | CENDAT24
       GND | 15                                                                         94 | VCCIO
    VCCINT | 16                                                                         93 | GND
  OUTDAT10 | 17                                                                         92 | OUTDAT11
FIRST_WORD | 18                                                                         91 | DATA12
   CENDAT2 | 19                              EP1K30TC144-1                              90 | CENDAT3
   CENDAT8 | 20                                                                         89 | OUTDAT15
  OUTDAT22 | 21                                                                         88 | OUTDAT18
  OUTDAT19 | 22                                                                         87 | FIRST
  OUTDAT12 | 23                                                                         86 | DATA10
     VCCIO | 24                                                                         85 | VCCINT
       GND | 25                                                                         84 | GND
   OUTDAT5 | 26                                                                         83 | CENDAT29
   OUTDAT4 | 27                                                                         82 | CENDAT11
       TP3 | 28                                                                         81 | CENDAT28
   CENDAT9 | 29                                                                         80 | OUTDAT29
    DATA15 | 30                                                                         79 | CENDAT14
  CENDAT27 | 31                                                                         78 | OUTDAT17
  CENDAT31 | 32                                                                         77 | ^MSEL0
   OUTDAT6 | 33                                                                         76 | ^MSEL1
      #TMS | 34                                                                         75 | VCCINT
  ^nSTATUS | 35                                                                         74 | ^nCONFIG
   CENDAT7 | 36                                                                         73 | DATA9
           |      38  40  42  44  46  48  50  52  54  56  58  60  62  64  66  68  70  72  _|
            \   37  39  41  43  45  47  49  51  53  55  57  59  61  63  65  67  69  71   |
             \---------------------------------------------------------------------------
                O T n G C C C C V O O O O V D G V P R n G G O C V O C C O G C O O O V L
                U P W N E E E E C U U U U C A N C H F C N N U E C U E E U N E U U U C 1
                T 1 R D N N N N C T T T T C T D C Y C L D D T N C T N N T D N T T T C _
                _   I   D D D D I D D D D I A   _ _ L E _   D D I D D D D   D D D D I A
                W   T   A A A A O A A A A N 0   C C K A C   A A O A A A A   A A A A O C
                E   E   T T T T   T T T T T     K R   R K   T T   T T T T   T T T T   C
                N       2 1 6 2   2 8 1 2       L       L   1 2   2 1 2 1   2 7 2 2   E
                        5 5   3   1   4 5       K       K   3 1   0 7 0 6   2   8 3   P
                                                                                      T
```

N.C. = No Connect. This pin has no internal connection to the device.
VCCINT = Dedicated power pin, which MUST be connected to VCC (2.5 volts).
VCCIO = Dedicated power pin, which MUST be connected to VCC (3.3 volts).
GND = Dedicated ground pin or unused dedicated input, which MUST be connected to GND.
RESERVED = Unused I/O pin, which MUST be left unconnected.

CHIP "zerosuppression" ASSIGNED TO AN EP1K30TC144-1

TCK	: 1
CONF_DONE	: 2
nCEO	: 3
TDO	: 4
VCCIO	: 5
GND	: 6
CENDAT0	: 7
CENDAT30	: 8
CENDAT13	: 9
CENDAT26	: 10
RDYnBUSY	: 11
OUTDAT2	: 12
DATA13	: 13
INIT_DONE	: 14
GND	: 15
VCCINT	: 16
OUTDAT10	: 17
FIRST_WORD	: 18
CENDAT2	: 19
CENDAT8	: 20
OUTDAT22	: 21
OUTDAT19	: 22
OUTDAT12	: 23
VCCIO	: 24
GND	: 25
OUTDAT5	: 26
OUTDAT4	: 27
TP3	: 28
CENDAT9	: 29
DATA15	: 30
CENDAT27	: 31
CENDAT31	: 32
OUTDAT6	: 33
TMS	: 34
nSTATUS	: 35
CENDAT7	: 36
OUT_WEN	: 37
TP1	: 38
nWRITE	: 39
GND	: 40
CENDAT25	: 41
CENDAT15	: 42
CENDAT6	: 43
CENDAT23	: 44
VCCIO	: 45
OUTDAT21	: 46
OUTDAT8	: 47
OUTDAT14	: 48
OUTDAT25	: 49
VCCINT	: 50
DATA0	: 51
GND	: 52
VCC_CKLK	: 53
PHY_CR	: 54
RFCLK	: 55
nCLEAR	: 56
GND_CKLK	: 57
GND	: 58
OUTDAT13	: 59
CENDAT21	: 60
VCCIO	: 61
OUTDAT20	: 62
CENDAT17	: 63

CENDAT20 : 64
OUTDAT16 : 65
GND : 66
CENDAT22 : 67
OUTDAT7 : 68
OUTDAT28 : 69
OUTDAT23 : 70
VCCIO : 71
L1_ACCEPT : 72
DATA9 : 73
nCONFIG : 74
VCCINT : 75
MSEL1 : 76
MSEL0 : 77
OUTDAT17 : 78
CENDAT14 : 79
OUTDAT29 : 80
CENDAT28 : 81
CENDAT11 : 82
CENDAT29 : 83
GND : 84
VCCINT : 85
DATA10 : 86
FIRST : 87
OUTDAT18 : 88
OUTDAT15 : 89
CENDAT3 : 90
DATA12 : 91
OUTDAT11 : 92
GND : 93
VCCIO : 94
CENDAT24 : 95
TP0 : 96
RESERVED : 97
CENDAT16 : 98
OUTDAT3 : 99
CENDAT18 : 100
CENDAT4 : 101
DATA14 : 102
VCCINT : 103
GND : 104
TDI : 105
nCE : 106
DCLK : 107
DATA0 : 108
DATA1 : 109
DATA2 : 110
DATA3 : 111
DATA4 : 112
DATA5 : 113
DATA6 : 114
VCCIO : 115
DATA7 : 116
OUTDAT1 : 117
DATA8 : 118
CENDAT19 : 119
OUTDAT27 : 120
OUTDAT31 : 121
DATA11 : 122
GND : 123
GND : 124
DEV_DS : 125
A02 : 126
VCCINT : 127
TP2 : 128
GND : 129
OUTDAT24 : 130
CENDAT12 : 131
OUTDAT0 : 132
OUTDAT30 : 133
VCCIO : 134
CENDAT10 : 135
OUTDAT9 : 136
CENDAT5 : 137
CENDAT1 : 138
GND : 139
OUTDAT26 : 140
nRS : 141
nWS : 142
CS : 143
nCS : 144