

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 5Ω bidirectional switches connect inputs to outputs
- Pin compatible with the 74F251, 74FCT251, and 74FCT251T
- Zero propagation delay, zero ground bounce
- TTL-compatible control inputs
- Undershoot clamp diodes on all switch and control pins
- Available in SOIC (S1), and QSOP

APPLICATIONS

- Logic replacement
- Video, audio, graphics switching, muxing
- Hot-swapping, hot-docking (Application Note AN-13)
- Voltage translation (5V to 3.3V; Application Note AN-11)

DESCRIPTION

The QS3251 is a high-speed CMOS TTL-compatible 8:1 multiplexer/demultiplexer. The QS3251 has 3-state outputs. The QS3251 is a function and pinout compatible version of the 74F251, 74FCT251 and the 74ALS/AS/LS251 8:1 multiplexers. The low ON resistance of the QS3251 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise.

Mux/Demux devices provide an order of magnitude faster speed than equivalent logic devices.

Figure 1. Functional Block Diagram

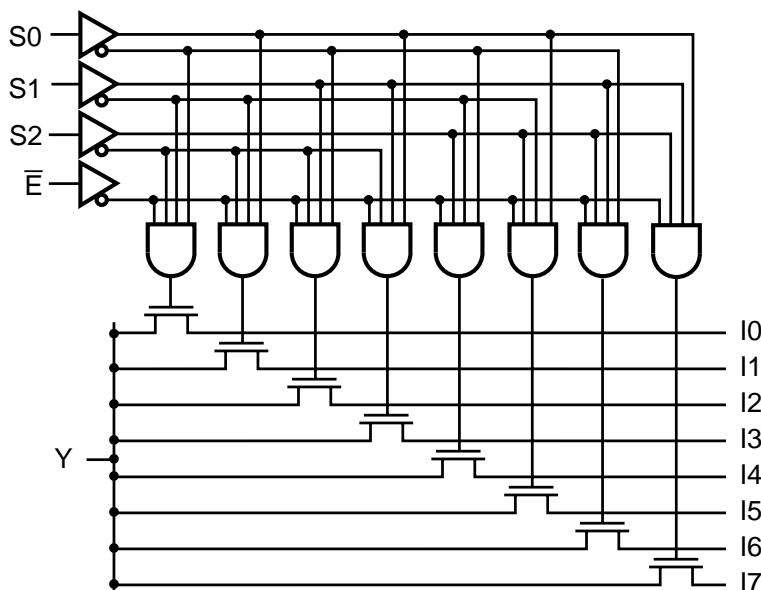


Table 1. Pin Description

Name	I/O	Description
I7-I0	I	Data Inputs
S2-S0	I	Select Inputs
\bar{E}	I	Enable Input
Y	O	Data Output

Table 2. Function Table

\bar{E}	Select			3251	Function
	S2	S1	S0	Y	
H	X	X	X	Hi-Z	Disable
L	L	L	L	I0	S2-S0 = 0
L	L	L	H	I1	S2-S0 = 1
L	L	H	L	I2	S2-S0 = 2
L	L	H	H	I3	S2-S0 = 3
L	H	L	L	I4	S2-S0 = 4
L	H	L	H	I5	S2-S0 = 5
L	H	H	L	I6	S2-S0 = 6
L	H	H	H	I7	S2-S0 = 7

**Figure 2. Pin Configuration
(All Pins Top View)**

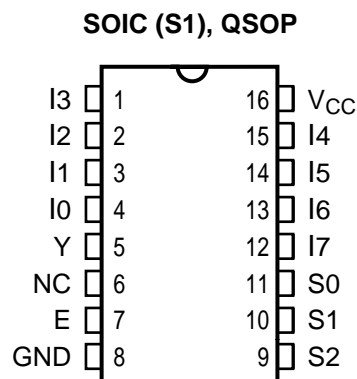


Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Switch Voltage V_S	-0.5V to +7.0V
DC Input Voltage V_{IN}	-0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins		SOIC, QSOP		Unit
		Typ	Max	
Control Inputs		4	5	pF
QuickSwitch Channels (Switch OFF)	Demux	5	7	pF
	Mux	21	23	pF

Note: Capacitance is guaranteed, but not production tested and are typical values. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

Table 5. DC Electrical Characteristics Over Operating Range

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
$ I_{IN} $	Input Leakage Current (Control Inputs)	$0\text{V} \leq V_{IN} \leq V_{CC}$	—	—	1	μA
$ I_{OZ} $	Off-State Current (Hi-Z)	$0\text{V} \leq V_{OUT} \leq V_{CC}$	—	—	1	μA
R_{ON}	Switch ON Resistance ⁽²⁾	$V_{CC} = \text{Min.}$, $V_{IN} = 0.0\text{V}$ $I_{ON} = 30\text{mA}$	—	5	7	Ω
R_{ON}	Switch ON Resistance ⁽²⁾	$V_{CC} = \text{Min.}$, $V_{IN} = 2.4\text{V}$ $I_{ON} = 15\text{mA}$	—	10	15	Ω
V_P	Pass Voltage ⁽³⁾	$V_{IN} = V_{CC} = 5\text{V}$, $I_{OUT} = -5\mu\text{A}$	3.7	4	4.2	V

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." R_{ON} guaranteed, but not production tested.
3. Pass voltage is guaranteed, but not production tested.

Figure 3. Typical ON Resistance vs. V_{IN} at $V_{CC} = 5.0\text{V}$

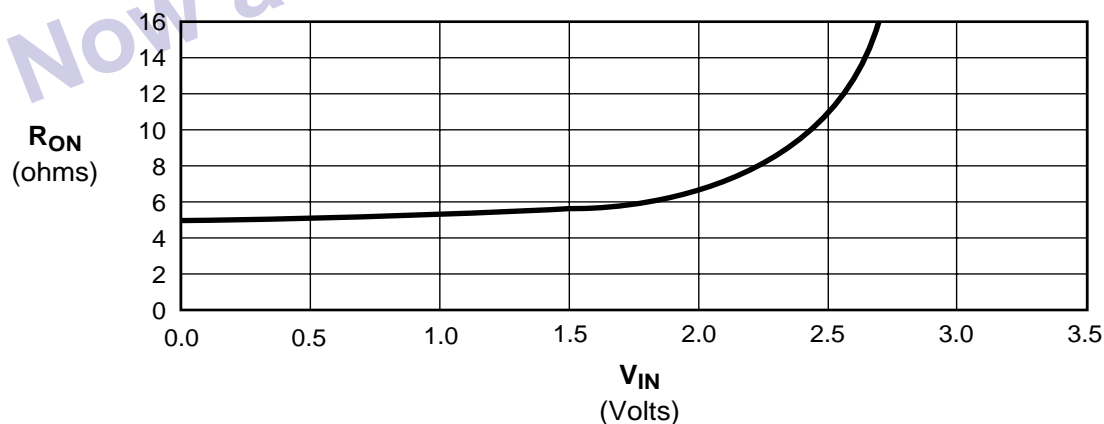


Table 6. Power Supply Characteristics Over Operating Range

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC} , $f = 0$	3	μA
ΔI_{CC}	Power Supply Current ⁽²⁾ per Input HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, $f = 0$ per Control Input	1.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz ⁽³⁾	$V_{CC} = \text{Max.}$, I and Y Pins Open, Controls Inputs Toggling @ 50% Duty Cycle	0.25	mA/MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$, control inputs only). I and Y pins do not contribute to ΔI_{CC} .
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

Table 7. Switching Characteristics Over Operating Range

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾	QS3251			Unit
		Min	Typ	Max	
t_{PLH} t_{PHL}	Data Propagation Delay ^(2,3) In to Y	—	—	0.25 ⁽³⁾	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay Sn to Y	0.5	—	6.6	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay ⁽²⁾ \bar{E} to Y	0.5	—	6.0	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay Sn, \bar{E} to Y	0.5	—	6.0	ns

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed, but not production tested.
2. This parameter is guaranteed, but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for $C_L = 50\text{pF}$. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.