# Specification of the MCCM Modules

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# 1. Introduction

The Muon Centroid Crate Manager (MCCM) is one of a set of VME cards used to form the Level 1 (L1) muon trigger decision for Run 2 of D0. A block diagram of the Muon Centroid (MC) VME crate is shown in F1. We presently envision a total of 4 such MC crates. The Muon Centroid Crate Manager can reside in the 1st slot of each of the MC crates, which are located on the D0 platform. The block diagram shows the standard MC crate configuration with 16 MCEN cards and an optional processor board ("Controller"). The MCEN modules correspond each to one octant within a given geographic region.

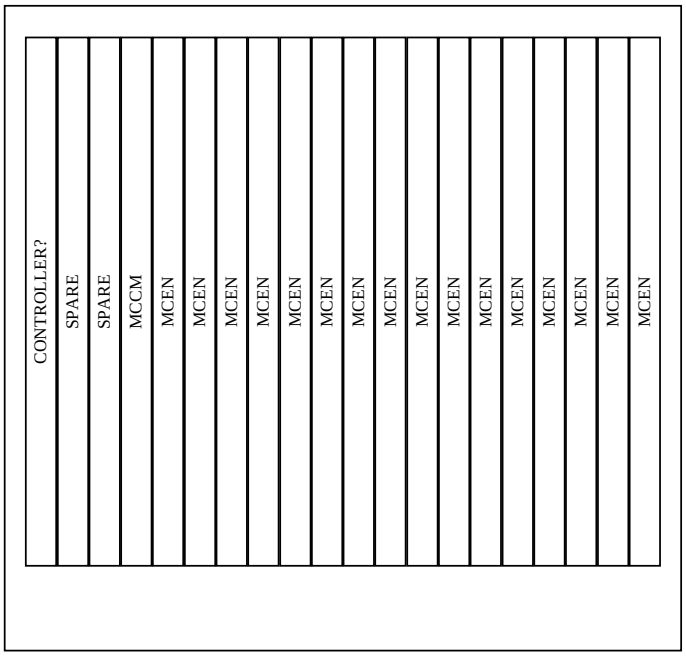


**Figure 1 — The MC Crate**

The configuration of the Muon Centroid Crate shown above is a typical configuration, showing all MCEN cards. It is possible for the crate to be used in many different configurations by changing the initialization from the processor board to the boards in the crate.

There are two types of input signals received by the MCCM from the outside world, timing and control. The timing signals such as the 53 MHz RF Clock, Reset and Sync Gap signals are connected to the MCCM through coax cable from the Muon Readout Card (MRC). The control signals, which include trigger accepts and rejects are connected to the MRC via a 50 pin twist and flat ribbon cable from the MRC.

The MCCM is constructed as a 9Ux400mm VME card and provides the following functions:

◊ Receives and decodes timing information from the MRC. These signals are the RF Clock, Reset, Sync Gap and Gap signals, The Sync Gap and Gap signals are decoded from one signal line from the MRC. The timing signals received by the MCCM are buffered and distributed to the MCEN cards. The Reset and Sync Gap signals arrive at the MCCM an arbitrary amount of time before the actual event in the accelerator turn. The MCCM adjusts its BC counter in such a way that the Reset signal is assigned the appropriate crossing number. That is, the Reset signal is assigned a preset BC number such that the BC number of the crossing in which the MCCM first sees data after the Sync Gap is **7**. This is described further in the timing section of this document. Thus the timing adjustment on the MCCM is to within

132 ns (1 BC). A finer timing adjustment takes place on the MTM card which sends the global muon trigger decision to the Trigger Framework (TF).

◊ Receives trigger information such as L1 ACCEPT, L2 ACCEPT and L2 REJECT, Bunch Crossing Number, etc. on a 50 conductor twist and flat cable from the MRC and passes this data to the MCEN cards in the crate.

◊ Upon receipt of an L1 ACCEPT signal the MCCM scans the MCEN modules for valid data, then reads the zero-suppressed centroid information from the MCEN memory. The MCCM then transmits all this data, along with the card status register, the card error register and an internally generated BC number, turn number and other header information to the L2 muon trigger.

◊ Upon receipt of an L2 ACCEPT the MCCM reads from each MCEN card its input data, card error and card status, raw centroid data and zero-suppressed centroid data. The MCCM then sends the above data, along with its own header data, BC number, turn number, etc., to the MRC for transfer to L3 via the VBD.

◊ The MCCM collects detected errors from itself and the MCEN cards, and sends an OR of these asynchronously to the MRC. Possible MCCM error conditions are discussed later.

◊ The MCCM collects Busy information for itself and each of the MCEN cards. A logical OR of these busy signals is sent as L1 BUSY to the trigger framework via the MRC.

◊ Upon receiving an initialization signal, the MCCM resets both the turn and BC number and clears all FIFOs and DPM pointer buffers on the MCEN cards and itself.

◊ The MCCM contains an interface to the 1553 system. Any VME Location in the MCCM crate can be written to (if not read-only) or read from via the 1553 controls system.

◊ The MCCM also contains a UART interface that mimics the 1553 system. Any VME Location in the MCCM crate can be written to (if not read-only) or read from via the UART controls system.

◊ The MCCM provides self test features to allow the board to generate its own L1 and L2 ACCEPT and reject signals that are normally supplied by the MRC. It also provides self-test features for the fast data transfer protocol through the backplane.

# *2. Inputs/Outputs*

## 2.1 VME Bus (J1 and J2 Connectors)

The MCCM has a VME interface using A32 addressing and is capable of up to 32 bit data transfers. The MCCM VMEbus controller has also master capability. It can also work as a slot 1 controller, providing bus arbitration and other master services.

## 2.2 Connections to MCEN Board (J2 Connector)

The J2 connector is used to communicate between the MCEN cards and MCCM. This connector is a 96 pin DIN type connector.

### 2.2.1 J2 Connections

The following is a list of the signals that exist on the J2 connector. For each signal, we have indicated the signal name, the type of signal (TTL, PECL, etc.), and the source and destination of the signal. Actual pin assignments for J2 can be found in Appendix A.

- ◊ M_CLOCK - (Differential PECL) - (from MCCM to MCENs) 4 differential signals that are distributed one for each pair of MCENs in the crate, this is the 53 MHz RF clock that is received from the MRC.

- ◊ BC_TRIG[0:7] - (TTL, terminated on backplane) - (from MCCM to MCENs) - This bus contains the BC Number to associate with the data when the L1-ACCEPT signal is active. Note that the BC Number is only 8 bits, the other 7 bits are not defined as of this revision.

- ◊ STORE_ALL - (TTL - terminated on backplane) - (from MCCM to MCENs) - This signal, which can only be active when L1 ACCEPT is active, indicates to the MCCMs that the data for the accepted BC needs to have all of its input data stored and made accessible to the VME bus for possible transmission to Level 3.

- ◊ L1 ACCEPT - (TTL, terminated on the backplane) - (from MCCM to MCENs) - Signal to indicate that the crate has received a L1 ACCEPT for the last trigger candidate sent to the Trigger Framework and all data should be saved. This signal comes a set number of crossings after the data is sent to the trigger framework, any candidate that does not receive an L1_ACCEPT is assumed to be rejected.

- ◊ SYNCH GAP - (TTL, terminated on the backplane) - (from MCCM to MCENs) - This signal indicates that the beam is in the synch Gap, which means that the input receiving FIFOs should be going empty with (??) clock signals. All of the input FIFOs must be emptied within the Gap, which will result in the INPUT_READY signal going high.

- ◊ INPUT_READY - (Open Collector TTL, pulled up on the MCCM) - (from MCENs to MCCM) - This signal is a “wire-or” that contains a high level signal when all of the MCENs in the crate have *empty* conditions in all of the input FIFOs that have not been masked off. If this signal does not go low during the synch Gap, this is an indication of an error condition to the MCCM.

- ◊ L2 ACCEPT - (TTL, terminated on the backplane) - (from MCCM to MCENs) - Signal to indicate that the Level 2 Trigger Framework has accepted a trigger candidate and that the address of the data should be made available in the Buffer Pointer FIFO.

- ◊ L2 REJECT - (TTL, terminated on the backplane) - (from MCCM to MCENs) - Signal to indicate that the Level 2 Trigger Framework has rejected the trigger candidate and that the buffer should be freed for use.

- ◊ DATA_READY* - (Open Collector TTL, pulled up on the MCCM) - (from MCENs to MCCM) - This signal is a “wire-or” that contains a low (asserted) level signal when some of the MCENs in the crate have L2 data ready to transfer to the MCCM. Each MCEN will release this signal when all of it’s active serial inputs, that have not been masked off on initialization, have received at least one byte of data and the card has sent its Card Trigger Data to the MCCM module.

- ◊ BC_CLOCK - (TTL, terminated on the backplane) - (From MCCM to MCENs) BC Clock created by the MCCM. This clock indicates a crate BC whenever the DATA_READY signal indicates that all MCENs have received valid data.

◊ LEVEL_1_BUSY* - (Open Collector TTL, pulled up on the MCCM) - “Wire-or” signal, each MCEN can cause this line to go low if there is a memory or FIFO full condition that would make it impossible for the board to process a L1 ACCEPT signal.

◊ LEVEL_2_BUSY* - (Open Collector TTL, pulled up on the MCCM) - “Wire-or” signal, each MCEN can cause this line to go low if there is a condition that make it impossible for the board to process an L2 ACCEPT signal.

◊ LEVEL_1_ERROR* - (Open Collector TTL, pulled up on the MCCM) - “Wire-or” signal, each MCEN can cause this line to go low if there is an error condition that needs to be reported to the MRC. This error could be caused by a mismatch between the expected and received BC Number for a L1 ACCEPT, L2 ACCEPT or L2 REJECT. This error could also be caused by an inoperative serial receiver on a MCEN Board.

◊ RESET_COUNTERS - (TTL, terminated on the backplane) - (from MCCM to MCENs) - Signal that causes the MCENs to reset their internal BC counters

◊ MASTER_RESET - (TTL, terminated on backplane) - (from MCCM to MCENs) - Master reset generated from the initialize command that causes all internal counters to be reset to initial condition.

◊ L2_MCEN_[15:0] – (TTL, terminated on backplane) – (from MCENs to MCCM) – Each of the modules will indicate, with one of these signals, if it has L2 data to be transferred to the MCCM. A brief sample of the bus in the beginning can indicate if there is at all any data. The bus will be priority encoded so that access is made to the modules that have useful data to be transferred.

◊ EOD* – (Open Collector TTL, pulled up on the MCCM) This signal is used at the end of a L3 data transfer. As all the modules are read, and have, potentially, different sizes of data, this line signals the MCCM that it can start addressing the next module.

◊ FAD[15:0]* – (TTL, terminated on the backplane) – (from the MCCM to the MCENs). Each MCEN in the crate has a predefined “fast address”, i.e. it can be addressed in a very fast way, without the need for time consuming address decoding. This allows a very fast change of addresses during L2 transfers, which is critical for a high performance transfer protocol.

◊ L3_HOLD – (TTL, terminated on the backplane) – (from the MCCM to the MCENs). If a L1 ACCEPT comes while the MCCM is transferring L3 Data, it asserts this line so that the transfer can be interrupted without much disruption. As soon as the accept is dealt with, this line is de-asserted and L3 data transfer continues from the point of interruption.

◊ TRGPROCENB – (TTL, terminated on the backplane) – (from the MCCM to the MCENs) . In order to prevent pile-up of events if two L1 or L2 ACCEPT signals reach the MCENs while a transfer is going on, this signal is asserted which prevents any change in the L2_MCEN[] lines, therefore preserving the event mask. As soon as the event is collected by the MCCM this line is de-asserted, and the MCCM will start dealing with the new data as soon as possible.

### 2.2.2 Data Formats

The MC system sends data to L1 directly from the MCEN modules, and to L2 and L3 from the MCCM. The various formats are indicated in a separate document.

### 2.2.3 MCCM Configuration and Status Registers

(still to be better described)

## 2.3 Serial Links

### 2.3.1 Serial Link to Level 2 Trigger Framework (L2_DATA)

Upon receipt of a Level 1 Accept, the following information is sent to the Level 2 muon preprocessor for use in the Level 2 muon trigger decision: MCEN card level centroid information (zero suppressed), status and error bits, counters, etc. The data is formatted according to 2.2.2.2.

This serial link, which is located in J3 and J4, operates at a word (2 bytes) rate of 16 MHz, resulting in a bit rate of 160 MHz, which means that it will take about 10 μs to transfer the data to Level 2 (exact time depends on the quantity of data) using two such links. This is much shorter than the required time of 100μs for the L1 acceptance rate of 10 kHz. This link is implemented using a Cypress HOTLink™ p/n CY7B923.

### 2.3.2 Serial Link to Level 3 Trigger Framework (L2_TRIG)

This serial link, located on J3, transfers the data that the MCCM has collected from each MCEN card when a L2 Accept is received. The MCCM collects the data from each MCEN using the VME Data Bus. The MCCM then formats the data (see 2.2.2.3.) and transmits it over the serial link.

The serial link will operate at a byte rate of 16 MHz, resulting in a serial clock rate of 160 MHz which means that it will take about 350 μs to transfer the data to Level 3. This is less than the required time of 1,000μs for the L2 acceptance rate of 1 kHz to give acceptance values. This link is implemented using a Cypress HOTLink™ p/n CY7B923.

## 2.4 Timing Signals

There are 3 signals that are used to synchronize the MCCM to the rest of the system. These signals originate at the Trigger Framework, are transported over the Serial Command Link to the Muon Fanout Card, distributed to the Muon Readout Cards over the VME backplane and sent via coaxial ASTRO cable to the MCCM. These signals must be adjusted digitally so that their relationship to the incoming data is correct. The correct relationship between the signals is shown in Figure 2.

- ◊ RF_Clock - 53 MHz Clock that is the basic accelerator RF signal.

- ◊ RESET - This signal indicates the beginning of a turn. The RESET signal is associated with the sixth bunch crossing before the first bunch crossing that contains real beam. The actual timing of the RESET signal on the MCCM is adjusted so that the data for the first bunch crossing that contains real beam is at the MCENs on bunch crossing 7. The amount of adjustment required will be determined during installation of the MCCM and will thereafter be checked by the MCCM and a Data Ready Error generated if the data is not arriving at the proper time. The MCCM also checks that the RESET pulse is occurring at the proper time with respect to it's internal counter and will report any discrepancy with a Reset Timing Error. This signal resets the BC number (but not the turn number). This signals also causes the internal Turn Number on the MCCM to be reset for the first RESET signal received after an INITIALIZE signal.

◊ SYNC_GAP - Signal to indicate an accelerator gap during which L1 Accepts are not permitted. These gaps are used to allow the input FIFOs to empty (and thus become synchronized later when they are all not empty). This gap also allows the logic to "catch up" after Level 1 accepts in the previous turn. Note that not all accelerator gaps will cause a GAP signal, some may be used for Cosmic Level 1 triggering. During the Synch Gap, all front ends will send idle signals (K28.5 as defined in the Fiber Channel specification) over their serial outputs to the MCENs which will maintain word synchronization at the MCEN. (Note: There is a possibility that this signal will be encoded, so that both Sync Gap and other Gaps may be identified, in which case the MCCM would check the location of both types of Gap but only uses the Sync Gap for it's internal logic purposes)

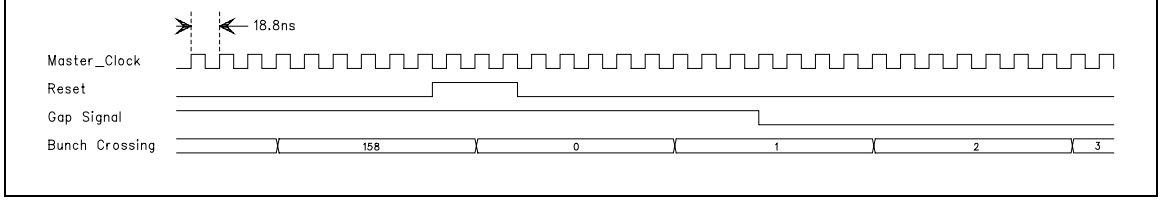


**Figure 2 - Reset and Gap Timing**

Another signal related to timing is INITIALIZE, which is sent over the 50 conductor cable from the MRC. When INITIALIZE is received at the MCCM, the serial links will send idles, after completing any messages that might be in progress when the INITIALIZE is received. INITIALIZE will reset all buffers and pointers and reset it's status and error registers. The Busy flag will be asserted until the initialization procedure in the MCCM is complete. The first RESET signal received after a power cycle or INITIALIZE signal is used to set the internal BC counter to the proper number and reset the turns counter, subsequent RESET signals are used to check that the BC counter is at the proper count when RESET is received, and to report an error if it is not.

The MCCM monitors the INPUT_READY and DATA_READY backplane signals to determine that they occur at the proper times, the measured times (in BC clock ticks) from receiving RESET to receiving INPUT_READY and DATA_READY is available in VME memory to the monitoring system and can be used for debugging purposes. INPUT_READY indicates when all unmasked inputs on all MCEN boards are not empty, and DATA_READY indicates when all MCEN boards have trigger decisions ready for transfer to the MCCM. These signals are obviously closely related and are included to simplify error detection and debugging.

### 2.5 MIL-STD-1553B / UART Connection

There is access to the memory of the crate via a MIL-STD-1553B port that is located on the front panel of the module. Details on using this port are contained in Appendix D.

Through this connection, the outside world can communicate with the crate. It can do the following:

- View/Modify memory locations – The 1553 / UART will be able to view the VMEbus and hence read or modify anything necessary.

- Select the mode of operation of the crate – During normal run times the crate does not use the VMEbus, so that a faster data transfer can occur. VMEbus is there, however, whenever the crate is initializing.

- Upload new FPGA configurations, as necessary (once modifications are done at least once, uploading might be necessary after each power-up cycle).

### 2.6 Parallel Link from MRC (J8)

There is a 50 conductor twist and flat cable that is used to communicate between the MCCM and the MRC using differential ECL signals. The pinouts for this connector are shown in Appendix C. Following is a list of the signals that are found on this cable.

◊ XING0 - XING7 - (from MRC to MCCM) - 8 bit number in the range of 1 to 159 that indicates the BC when the L1 Accept signal is active

◊ INITIALIZE - (from MRC to MCCM) - This signal causes all internal registers, memories and FIFOs to be cleared, except for error registers, which are maintained until read. The error registers will be read out through the internal UART after being polled by the control system. INITIALIZE may also cause other reset sequences, such as using the Built In Self Test feature of the outgoing serial links to L2 and L3, and will maintain a BUSY state until all such sequences are completed and the error registers are read out if set.

◊ L1_ACCEPT - (from MRC to MCCM) - Signal indicates that the BC number contained in XING0 to XING7 was accepted. All data associated with this crossing will be maintained (both in the MCCM and the MCENs) and the L2_DATA message described in 2.3.2 will be transmitted.

◊ L2_ACCEPT - (from MRC to MCCM) - Signal indicates that the next BC number awaiting a L2 decision (i.e. a BC that has previously had a L1_ACCEPT) has been accepted. The MCCM determines if this is a 1 of n acceptance and sends the full L2_TRIG described in 2.3.3 if it is or a truncated message if it is not. After collecting the data for this transfer from each MCEN, the MCCM frees the buffer area in each MCCM that had been used for this event, as well as it's own buffer area.

◊ L2_REJECT - (from MRC to MCCM) - Signal indicates that the next BC number awaiting a L2 decision (i.e. a BC that has previously had a L1_ACCEPT) has been rejected. The MCCM informs the MCENs, which causes them to clear their buffers, and clears it's own buffer for this BC.

◊ UART_XMIT - (from MRC to MCCM) - Serial communications line from MRC. Normally used to request error transmission during initialization process, but can be used for other control functions.

◊ BUFFER_AVAILABLE - (from MRC to MCCM) - Used to indicate that the MRC has buffer space available to accept the L2_TRIG data required after a L2_ACCEPT is received. If this line is not high, the MCCM will hold the L2_TRIG Data until the line goes high and the data can be sent to the MRC.

◊ STROB - (from MRC to MCCM) - Strobe signal used to time all data from the MRC, data is valid on rising edge of this signal.

◊ UART_RCV - (from MRC to MCCM) - Serial communications line to the MRC. Normally used to transmit error codes when requested by MRC, but can also be used for other control functions. This signal will never transmit, except when requested to with an appropriate command sent over the UART_XMIT line.

◊ LEVEL_1_ERROR - (from MCCM to MRC) - This signal indicates that a Level 1 error has been detected in the crate. Level 1 errors may be caused by bad serial links, mismatched BC counters, VME bus error, or other detectable errors. This is a latched signal that will stay active once set until an INITIALIZE signal is received. The cause of this error is also latched and will not be reset until the error register is read out during the initialization process..

◊ LEVEL_1_BUSY - (from MRC to MCCM) - This signal indicates that a FIFO or memory associated with an input is full (or possibly within 1 accept cycle of becoming full) and that the crate can process no more L1_ACCEPTS until this signal goes low. This signal will also become active upon Initialization and will stay active if it has internal stored errors until the error are read out by the UART.

◊ LEVEL_2_BUSY - (from MCCM to MRC) - This signal indicates that the MCCM can process no more L2 accepts, at this writing there are no known cases that can cause this condition.

# *3. Front Panel Indicators and Switches*

## 3.1 Front Panel Indicators

◊ Power On (Green)

◊ +5v Power Supply Good (Green)

◊ +3.3v Power Supply Good (Green)

◊ -12v Power Supply Good (Green)

◊ Receiver Error (Red)

◊ Memory Error (Red)

◊ L1 Accept (Green)

◊ L1 Reject (Red) (absence of L1_Accept)

◊ L2 Accept (Green)

◊ L2 Reject (Red)

◊ L2 Readout (scaled) (series of LED’s in sequence)

◊ L3 Readout (scaled) (series of LED’s in sequence)

◊ Crossing Error Mismatch (Red)

◊ Sync Number Error (Red)

◊ Reset Time Error (Red)

◊ Sync Gap Time Error (Red)

- ◊ Data Ready Error (Red)
- ◊ MCCM BC Batch Error (Red)
- ◊ MCEN Error (Red)
- ◊ VME Error (Red)
- ◊ 1553B Interface Active

### 3.2 Front Panel Switches

There are no Front Panel Switches

### 3.3 Front Panel Connectors

The MCCM will have the following connectors on the front panel:

- MIL-STD-1553B
- J8 (to MRC)

# Appendix A — The J1 Connector

| J1 Connections | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Label | Pin | Label | Pin | Label | Pin | Label | Pin | Label |
| Z1 | BUS | A1 | D00 | B1 | BBSY* | C1 | D08 | D1 | BUS |
| Z2 | **GND** | A2 | D01 | B2 | BCLR* | C2 | D09 | D2 | **GND** |
| Z3 | BUS | A3 | D02 | B3 | ACFAIL* | C3 | D10 | D3 | BUS |
| Z4 | **GND** | A4 | D03 | B4 | BG0IN* | C4 | D11 | D4 | BUS |
| Z5 | BUS | A5 | D04 | B5 | BG0OUT* | C5 | D12 | D5 | BUS |
| Z6 | **GND** | A6 | D05 | B6 | BG1IN* | C6 | D13 | D6 | BUS |
| Z7 | BUS | A7 | D06 | B7 | BG1OUT* | C7 | D14 | D7 | BUS |
| Z8 | **GND** | A8 | D07 | B8 | BG2IN* | C8 | D15 | D8 | BUS |
| Z9 | BUS | A9 | **GND** | B9 | BG2OUT* | C9 | **GND** | D9 | GAP* |
| Z10 | **GND** | A10 | SYSCLK | B10 | BG3IN* | C10 | SYSFAIL* | D10 | GA0* |
| Z11 | BUS | A11 | **GND** | B11 | BG3OUT* | C11 | BERR* | D11 | GA1* |
| Z12 | **GND** | A12 | DS1* | B12 | BR0* | C12 | SYSRESET* | D12 | **3.3V** |
| Z13 | BUS | A13 | DS0* | B13 | BR1* | C13 | LWORD* | D13 | GA2* |
| Z14 | **GND** | A14 | WRITE* | B14 | BR2* | C14 | AM5 | D14 | **3.3V** |
| Z15 | BUS | A15 | **GND** | B15 | BR3* | C15 | A23 | D15 | GA3* |
| Z16 | **GND** | A16 | DTACK* | B16 | AM0 | C16 | A22 | D16 | **3.3V** |
| Z17 | BUS | A17 | **GND** | B17 | AM1 | C17 | A21 | D17 | GA4* |
| Z18 | **GND** | A18 | AS* | B18 | AM2 | C18 | A20 | D18 | **3.3V** |
| Z19 | BUS | A19 | **GND** | B19 | AM3 | C19 | A19 | D19 | BUS |
| Z20 | **GND** | A20 | IACK* | B20 | **GND** | C20 | A18 | D20 | **3.3V** |
| Z21 | BUS | A21 | IACKIN* | B21 | SERA | C21 | A17 | D21 | BUS |
| Z22 | **GND** | A22 | IACKOUT* | B22 | SERB | C22 | A16 | D22 | **3.3V** |
| Z23 | BUS | A23 | AM4 | B23 | GND | C23 | A15 | D23 | BUS |
| Z24 | **GND** | A24 | A07 | B24 | IRQ7* | C24 | A14 | D24 | **3.3V** |
| Z25 | BUS | A25 | A06 | B25 | IRQ6* | C25 | A13 | D25 | UNT. BUS |
| Z26 | **GND** | A26 | A05 | B26 | IRQ5* | C26 | A12 | D26 | **3.3V** |
| Z27 | BUS | A27 | A04 | B27 | IRQ4* | C27 | A11 | D27 | UNT. BUS |
| Z28 | **GND** | A28 | A03 | B28 | IRQ3* | C28 | A10 | D28 | **3.3V** |
| Z29 | BUS | A29 | A02 | B29 | IRQ2* | C29 | A09 | D29 | BUS |
| Z30 | **GND** | A30 | A01 | B30 | IRQ1* | C30 | A08 | D30 | **3.3V** |
| Z31 | BUS | A31 | **-12V** | B31 | **+5VSTDBY** | C31 | **+12V** | D31 | **GND** |
| Z32 | **GND** | A32 | **+5V** | B32 | **+5V** | C32 | **+5V** | D32 | BUS |

NC: Not Connected.
BUS: Bussed Line

# Appendix A — J2 Connections

| J1 Connections | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Pin | Label | Pin | Label | Pin | Label | Pin | Label | Pin | Label |
| Z1 | **+5V** | A1 | M_CLOCK+0 | B1 | **+5V** | C1 | M_CLOCK-0 | D1 | **GND** |
| Z2 | **GND** | A2 | M_CLOCK+1 | B2 | **GND** | C2 | M_CLOCK-1 | D2 | FAD0 |
| Z3 | **+5V** | A3 | M_CLOCK+2 | B3 | RETRY* | C3 | M_CLOCK-2 | D3 | **GND** |
| Z4 | **GND** | A4 | M_CLOCK+3 | B4 | A24 | C4 | M_CLOCK-3 | D4 | FAD1 |
| Z5 | **+5V** | A5 | M_RESET | B5 | A25 | C5 | RESET_COUNTERS | D5 | **GND** |
| Z6 | **GND** | A6 | STORE_ALL | B6 | A26 | C6 | LEVEL_1_BUSY* | D6 | FAD2 |
| Z7 | **+5V** | A7 | SYNCH_GAP | B7 | A27 | C7 | LEVEL_2_BUSY* | D7 | **GND** |
| Z8 | **GND** | A8 | DATA_READY* | B8 | A28 | C8 | LEVEL_1_ERROR* | D8 | FAD3 |
| Z9 | **+5V** | A9 | **GND** | B9 | A29 | C9 | **GND** | D9 | **GND** |
| Z10 | **GND** | A10 | BC_Trig0 | B10 | A30 | C0 | BC_Trig1 | D10 | FAD4 |
| Z11 | **+5V** | A11 | BC_Trig2 | B11 | A31 | C1 | BC_Trig3 | D11 | **GND** |
| Z12 | **GND** | A12 | BC_Trig4 | B12 | **GND** | C2 | BC_Trig5 | D12 | FAD5 |
| Z13 | **+5V** | A13 | BC_Trig6 | B13 | **+5V** | C3 | BC_Trig7 | D13 | **GND** |
| Z14 | **GND** | A14 | **GND** | B14 | D16 | C4 | **GND** | D14 | FAD6 |
| Z15 | **+5V** | A15 | **+5V** | B15 | D17 | C5 | **+5V** | D15 | **GND** |
| Z16 | **GND** | A16 | L1_ACCEPT | B16 | D18 | C16 | TRST* | D16 | FAD7 |
| Z17 | **+5V** | A17 | L2_ACCEPT | B17 | D19 | C17 | TDI | D17 | **GND** |
| Z18 | **GND** | A18 | L2_REJECT | B18 | D20 | C18 | TDO | D18 | FAD8 |
| Z19 | **+5V** | A19 | BC_CLOCK | B19 | D21 | C19 | TMS | D19 | **GND** |
| Z20 | **GND** | A20 | L3_HOLD | B20 | D22 | C20 | TCLK | D20 | FAD9 |
| Z21 | **+5V** | A21 | TRGPROCENB | B21 | D23 | C21 | EOD* | D21 | **GND** |
| Z22 | **GND** | A22 | **GND** | B22 | **GND** | C22 | **GND** | D22 | FAD10 |
| Z23 | **+5V** | A23 | L2_MCEN_8 | B23 | D24 | C23 | L2_MCEN_0 | D23 | **GND** |
| Z24 | **GND** | A24 | L2_MCEN_9 | B24 | D25 | C24 | L2_MCEN_1 | D24 | FAD11 |
| Z25 | **+5V** | A25 | L2_MCEN_10 | B25 | D26 | C25 | L2_MCEN_2 | D25 | **GND** |
| Z26 | **GND** | A26 | L2_MCEN_11 | B26 | D27 | C26 | L2_MCEN_3 | D26 | FAD12 |
| Z27 | **+5V** | A27 | L2_MCEN_12 | B27 | D28 | C27 | L2_MCEN_4 | D27 | **GND** |
| Z28 | **GND** | A28 | L2_MCEN_13 | B28 | D29 | C28 | L2_MCEN_5 | D28 | FAD13 |
| Z29 | **+5V** | A29 | L2_MCEN_14 | B29 | D30 | C29 | L2_MCEN_6 | D29 | **GND** |
| Z30 | **GND** | A30 | L2_MCEN_15 | B30 | D31 | C30 | L2_MCEN_7 | D30 | FAD14 |
| Z31 | **+5V** | A31 | **GND** | B31 | **GND** | C31 | **GND** | D31 | **GND** |
| Z32 | **GND** | A32 | **+5V** | B32 | **+5V** | C32 | **+5V** | D32 | FAD15 |

# Appendix B — J3 and J4 Connections (MRC)

| J3 Connections (Link 1) | | | |
|---|---|---|---|
| Pin | Label | Pin | Label |
| 1 | L2_DATA1+ | 2 | L2_DATA1- |
| 3 | RF_CLOCK+ | 4 | RF_CLOCK- |
| 5 | L2_TRIG+ | 6 | L2_TRIG- |
| 7 | ENC_TIMING+ | 8 | ENC_TIMING- |

| J4 Connections (Link 2) | | | |
|---|---|---|---|
| Pin | Label | Pin | Label |
| 1 | L2_DATA2+ | 2 | L2_DATA2- |
| 3 | RF_CLOCK+ | 4 | RF_CLOCK- |
| 5 | L2_TRIG+ | 6 | L2_TRIG- |
| 7 | ENC_TIMING+ | 8 | ENC_TIMING- |

# Appendix C — J8 Connections (MRC)

| J8 Connections | | | |
|---|---|---|---|
| Pin | Label | Pin | Label |
| 1 | XING1+ | 2 | XING1- |
| 3 | XING2+ | 4 | XING2- |
| 5 | XING3+ | 6 | XING3- |
| 7 | XING4+ | 8 | XING4- |
| 9 | XING5+ | 10 | XING5- |
| 11 | XING6+ | 12 | XING6- |
| 13 | XING7+ | 14 | XING7- |
| 15 | XING8+ | 16 | XING8- |
| 17 | INITIALIZE+ | 18 | INITIALIZE- |
| 19 | L1_ACCEPT+ | 20 | L1_ACCEPT- |
| 21 | | 22 | |
| 23 | L2_ACCEPT+ | 24 | L2_ACCEPT- |
| 25 | L2_REJECT+ | 26 | L2_REJECT- |
| 27 | UART_XMIT+ | 28 | UART_XMIT- |
| 29 | DONE+ | 30 | DONE- |
| 31 | STROB+ | 32 | STROB- |
| 33 | UART_RCV+ | 34 | UART_RCV- |
| 35 | LEVEL_1_ERROR+ | 36 | LEVEL_1_ERROR- |
| 37 | LEVEL_1_BUSY+ | 38 | LEVEL_1_BUSY- |
| 39 | LEVEL_2_BUSY+ | 40 | LEVEL_2_BUSY- |
| 41 | GND | 42 | GND |
| 43 | GND | 44 | GND |
| 45 | GND | 46 | GND |
| 47 | GND | 48 | GND |
| 49 | GND | 50 | GND |

# Appendix D — MIL-STD-1553B

(see “1553 Communications in the Level 1 Muon Trigger System”, by KJ and JS for more updated specs. What follows is a description of the previous system)

All Commands to the MCCM received over the MIL-STD-1553B serial link will consist of a 1553B Control Word followed by a Data Word that the UAZ1553 test board will interpret as a Command Word. The meaning of the Command Word is shown in Table F3. These 2 words may be followed by up to 30 Data Words whose meaning will vary depending on the Command Word. The 1553B Control word is defined in the MIL-STD-1553B spec. It will have the address of the UAZ1553 test board in bits 4-8 (this can be thought of as the crate address), bit 9 will indicate if the 1553B is sending or requesting data, bits 10-14 (normally the sub-address) are ignored, and bits 15-19 will contain the number of words to be transferred (0-31). Bits 0-3 are Sync bits, and bit 20 is a parity bit. Sync and parity are handled in hardware.

All data that is received from the MIL-STD-1553B bus is made available to a PIC micro-controller. The PIC will interpret the data (when necessary) and cause the proper action to occur. RC0 through RC7 on the PIC are used as a bi-directional data bus to transfer data between the PIC and the 1553B interface circuit. The rest of the bits are defined below:

RTCC - DATA_READY - (I/F => PIC) - Rising edge indicates that the data on the bus is the first byte of a received control or data word. (unless SET_BYTE_1/2 is high).

RB0 - VME_ERROR - (I/F => PIC) - Indicates a VME time-out has occurred.

RB1 - CONTROL/DATA - (I/F => PIC) - Valid when DATA_READY is high. Indicates if the data is a control word or data.

RB2 - PARITY_ERROR - (I/F => PIC) - Valid when DATA_READY is high. Indicates parity error on received word.

RB3 - 1553_XMIT_DONE - (I/F => PIC) - High indicates 1553 Transmit is completed.

RB4 - NC.

RB5 - STROBE - (PIC => I/F) - Latches a byte into or out of 1553 interface. Direction depends on state of R/W signal..

RB6 - NC.

RB7 - STATUS_LED - Indicates that the 1553 interface board is addressed to listen or talk. It is also illuminated after a PIC reset and remains on until the board is addressed

RA0 - SELECT_0- Select VME Interface and Control function. See table E1.

RA1 - SELECT_1- Select VME Interface and Control function. See table E1.

RA2 - SELECT_2- Select VME Interface and Control function. See table E1.

RA3 - SELECT_3- Select VME Interface and Control function. See table E1.

**Table F1 : "VME Interface and Control" FPGA functions**

| SELECT_3 | SELECT_2 | SELECT_1 | SELECT_0 | Function Selected |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | PIC wants 1553 RT listen address placed on INT_D bus. PIC will pulse STROBE high to acknowledge (VME interface FPGA ==> PIC) |
| 0 | 0 | 0 | 1 | Transmit stored message as a 1553 Control Word |
| 0 | 0 | 1 | 0 | Transmit stored message as a 1553 Data Word |
| 0 | 0 | 1 | 1 | Set High order VME address. ( PIC ==> VME interface FPGA) |
| 0 | 1 | 0 | 0 | Set Middle VME address. ( PIC ==> VME interface FPGA) |
| 0 | 1 | 0 | 1 | Set Low order VME address. ( PIC ==> VME interface FPGA) |
| 0 | 1 | 1 | 0 | Read in VME memory. (1553Rx ==> VME) Data in 1553 Receive Register is stored in VME memory at location indicated by address pointer. |
| 0 | 1 | 1 | 1 | Write out VME memory. ( VME ==> 1553Tx) VME memory contents indicated by address pointer are written to the 1553 Transmit Buffer. |
| 1 | 0 | 0 | 0 | Reset VME bus and light VME_ERROR LED |
| 1 | 0 | 0 | 1 | Turn off VME_ERROR LED |
| 1 | 0 | 1 | 0 | Read Byte 1. (1553Rx ==> PIC) Strobe in the low order byte into the PIC. |
| 1 | 0 | 1 | 1 | Write Byte 1. (PIC ==> 1553Tx) Strobe the low order byte into the 1553 transmit buffer. |
| 1 | 1 | 0 | 0 | Read Byte 2. (1553Rx ==> PIC) Strobe in the high order byte into the PIC. |
| 1 | 1 | 0 | 1 | Write Byte 2 (PIC ==> 1553Tx) Strobe the high order byte into the 1553 transmit buffer. |
| 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 1 | Initiates an interrupt that Resets the Crate Processor. |

**Table F2: UAZ1553 Interface Board Command Word format**

| Bits | Function |
|---|---|
| 15..08 | Basic Command. See table below for a description of the Basic commands that are recognized by the Interface Board. Reception of an unknown command will result in the entire transmission being ignored |
| 07..00 | Not Used |

The "Interface Board Command Word" is always the first data word received in a 1553 data transmission.

**Table F3: UAZ1553 INTERFACE BOARD COMMAND WORD**

| Basic Command Bits 15..08 | Description |
|---|---|
| 00h | Indicates a transfer of data into VME Memory at the present address. MCCM increments low order address bits for each data word transferred. |
| 01h | Indicates a transfer of data out of VME Memory from the present address. MCCM increments low order address bits for each data word transferred. |
| 02h | Initiates an interrupt that causes Crate Processor to reset |
| 03h | Set VME Address - Resets the 24 bit VME address to the contents of the next 2 data transfers. |

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# Appendix E — VME Memory Maps

These memory maps assume a 5-bit user defined Base Address, formed from bits 27 to 31 of the address lines.

| System and MCCM Memory Locations | |
|---|---|
| Memory Address | Description |
| 000000 - 00001E | Configuration Registers |
| 000020 - 00003E | Status Registers |
| 000040 | Number of MCEN modules in crate |
| 000042 | Address of MCEN #1 FPGA Data |
| 000044 | Size of MCEN #1 FPGA Data |
| 000046 | CRC of MCEN #1 FPGA Data |
| 000048 | Address of MCEN #2 FPGA Data |
| 00004A | Size of MCEN #2 FPGA Data |
| 00004C | CRC of MCEN #2 FPGA Data |
| 00004E | Address of MCEN #3 FPGA Data |
| 000050 | Size of MCEN #3 FPGA Data |
| 000052 | CRC of MCEN #3 FPGA Data |
| 000054 | Address of MCEN #4 FPGA Data |
| 000056 | Size of MCEN #4 FPGA Data |
| 000058 | CRC of MCEN #4 FPGA Data |
| 00005A | Address of MCEN #5 FPGA Data |
| 00005C | Size of MCEN #5 FPGA Data |
| 00005E | CRC of MCEN #5 FPGA Data |
| 000060 | Address of MCEN #6 FPGA Data |
| 000062 | Size of MCEN #6 FPGA Data |
| 000064 | CRC of MCEN #6 FPGA Data |
| 000066 | Address of MCEN #7 FPGA Data |
| 000068 | Size of MCEN #7 FPGA Data |
| 00006A | CRC of MCEN #7 FPGA Data |
| 00006C | Address of MCEN #8 FPGA Data |
| 00006E | Size of MCEN #8 FPGA Data |
| 000070 | CRC of MCEN #8 FPGA Data |
| 000072 | Address of MCEN #9 FPGA Data |

| System and MCCM Memory Locations | |
|---|---|
| 000074 | Size of MCEN #9 FPGA Data |
| 000076 | CRC of MCEN #9 FPGA Data |
| 000078 | Address of MCEN #10 FPGA Data |
| 00007A | Size of MCEN #10 FPGA Data |
| 00007C | CRC of MCEN #10 FPGA Data |
| 00007E | Address of MCEN #11 FPGA Data |
| 000080 | Size of MCEN #11 FPGA Data |
| 000082 | CRC of MCEN #11 FPGA Data |
| 000084 | Address of MCEN #12 FPGA Data |
| 000086 | Size of MCEN #12 FPGA Data |
| 000088 | CRC of MCEN #12 FPGA Data |
| 00008A | Address of MCEN #13 FPGA Data |
| 00008C | Size of MCEN #13 FPGA Data |
| 00008E | CRC of MCEN #13 FPGA Data |
| 000090 | Address of MCEN #14 FPGA Data |
| 000092 | Size of MCEN #14 FPGA Data |
| 000094 | CRC of MCEN #14 FPGA Data |
| 000096 | Address of MCEN #15 FPGA Data |
| 000098 | Size of MCEN #15 FPGA Data |
| 00009A | CRC of MCEN #15 FPGA Data |
| 00009C | Address of MCEN #16 FPGA Data |
| 00009E | Size of MCEN #16 FPGA Data |
| 0000A0 | CRC of MCEN #16 FPGA Data |
| 0000A2 - 0000FF | Undefined |
| 000100 - 3FFFFF | MCEN FPGA Data Memory |
| 400000 - 7FFFFF | Test And Pattern Area, tbd. |