Muon Centroid System Backplane Definition

by Emanuel Machado
1/7/99

Introduction

Being essentially a custom system, we want the MC to be able to be read and written to using VMEbus. This capitalizes on the large number of memory and CPU modules available that can be used to monitor, test and control the system.

However, we need extra flexibility due to the data rate requirements by the experiment. For that purpose, the following backplane is used.

Requirements

We require, from this backplane, the following features:

- Must be able to hold large amount of power. Extra power pins will be needed.
- Must allow very high speeds (reduced or suppressed reflections and ringing)
- Must be quiet at very high speeds
- Must be able to hold all the necessary trigger and control signals
- Must be VME compatible
- Must be cost effective
- Must use, in a 9U crate, only J1 and J2
- Must provide EMI/RFI shielding.

Technology

One of the limitations of current backplanes, is that they need to be considered a set of transmission lines. Because of that, reflections and ringing are factors that determine the performance of the backplane, limiting its maximum frequency. Other important factors are power distribution and crosstalk, which are typically solved using multilayer backplanes with heavy ground and power planes.

Bustronic, Inc. demonstrated recently a backplane capable of rates as high as 320 MB/s, while maintaining VMEbus compatibility. This special backplane circumvents the transmission line problem by making it appear as a capacitative lumped load. This allows to use incident wave switching, and supports source synchronous data transfers (SST). This method of transfer allows reliable high-frequency switching, which then allows for high data rates.

The crosstalk, measured at the noisiest signals, is less than 250 mV. The great news is that this backplane has a price tag comparable to the standard VME64 backplanes. This backplane is monolithic, i.e. includes J1 and J2.

Due to these attractive technological characteristics, we choose to use a variation of the Bustronic VME320 backplane **P/N 101V320M21-2500**. This will allow us to transfer, using a frequency of RF/2 (26.5 MHz), 106 MB/s in 32-bit words, or 212 MB/s in 64-bit words.

The J1 Connector

J1, in the MC system, is totally dedicated to VMEbus. It is a DIN41612 Enhanced Type C Eurocard connector (Harting, Inc. VME64 160 pins), which adds more ground connections between board and connector. Its pinout is, then, the following:

J1 Connections									
Pin	Label	Pin	Label	Pin	Label	Pin	Label	Pin	Label
Z1	BUS	A1	D00	B1	BBSY*	C1	D08	D1	BUS
Z2	**GND**	A2	D01	B2	BCLR*	C2	D09	D2	**GND**
Z3	BUS	A3	D02	B3	ACFAIL*	C3	D10	D3	BUS
Z4	**GND**	A4	D03	B4	BG0IN*	C4	D11	D4	BUS
Z5	BUS	A5	D04	B5	BG0OUT*	C5	D12	D5	BUS
Z6	**GND**	A6	D05	B6	BG1IN*	C6	D13	D6	BUS
Z7	BUS	A7	D06	B7	BG1OUT*	C7	D14	D7	BUS
Z8	**GND**	A8	D07	B8	BG2IN*	C8	D15	D8	BUS
Z9	BUS	A9	**GND**	B9	BG2OUT*	C9	**GND**	D9	GAP*
Z10	**GND**	A10	SYSCLK	B10	BG3IN*	C10	SYSFAIL*	D10	GA0*
Z11	BUS	A11	**GND**	B11	BG3OUT*	C11	BERR*	D11	GA1*
Z12	**GND**	A12	DS1*	B12	BR0*	C12	SYSRESET*	D12	**3.3V**
Z13	BUS	A13	DS0*	B13	BR1*	C13	LWORD*	D13	GA2*
Z14	**GND**	A14	WRITE*	B14	BR2*	C14	AM5	D14	**3.3V**
Z15	BUS	A15	**GND**	B15	BR3*	C15	A23	D15	GA3*
Z16	**GND**	A16	DTACK*	B16	AM0	C16	A22	D16	**3.3V**
Z17	BUS	A17	**GND**	B17	AM1	C17	A21	D17	GA4*
Z18	**GND**	A18	AS*	B18	AM2	C18	A20	D18	**3.3V**
Z19	BUS	A19	**GND**	B19	AM3	C19	A19	D19	BUS
Z20	**GND**	A20	IACK*	B20	**GND**	C20	A18	D20	**3.3V**
Z21	BUS	A21	IACKIN*	B21	SERA	C21	A17	D21	BUS
Z22	**GND**	A22	IACKOUT*	B22	SERB	C22	A16	D22	**3.3V**
Z23	BUS	A23	AM4	B23	GND	C23	A15	D23	BUS
Z24	**GND**	A24	A07	B24	IRQ7*	C24	A14	D24	**3.3V**
Z25	BUS	A25	A06	B25	IRQ6*	C25	A13	D25	UNT. BUS
Z26	**GND**	A26	A05	B26	IRQ5*	C26	A12	D26	**3.3V**
Z27	BUS	A27	A04	B27	IRQ4*	C27	A11	D27	UNT. BUS
Z28	**GND**	A28	A03	B28	IRQ3*	C28	A10	D28	**3.3V**
Z29	BUS	A29	A02	B29	IRQ2*	C29	A09	D29	BUS
Z30	**GND**	A30	A01	B30	IRQ1*	C30	A08	D30	**3.3V**
Z31	BUS	A31	**-12V**	B31	**+5VSTDBY**	C31	**+12V**	D31	**GND**
Z32	**GND**	A32	**+5V**	B32	**+5V**	C32	**+5V**	D32	BUS

Figure 1 – The J1 Connector

NC: Not Connected.
BUS: Bussed Line

The J2 Connector

The J2 Connector gives 32-bit data possibility to VMEbus, and adds 64 User Defined pins. These will be used, in our application, as shown below. It is a DIN41612 Enhanced Type C Eurocard connector (Harting, Inc. VME64 160 pins), which adds more ground connections between board and connector.

All pins in rows A and C are bussed, except for the extra power and ground pins, that should be connected directly to the power and ground planes.

J1 Connections									
Pin	Label	Pin	Label	Pin	Label	Pin	Label	Pin	Label
Z1	**+5V**	A1	M_CLOCK+0	B1	**+5V**	C1	M_CLOCK-0	D1	**GND**
Z2	**GND**	A2	M_CLOCK+1	B2	**GND**	C2	M_CLOCK-1	D2	FAD0
Z3	**+5V**	A3	M_CLOCK+2	B3	RETRY*	C3	M_CLOCK-2	D3	**GND**
Z4	**GND**	A4	M_CLOCK+3	B4	A24	C4	M_CLOCK-3	D4	FAD1
Z5	**+5V**	A5	M_RESET	B5	A25	C5	RESET_COUNTERS	D5	**GND**
Z6	**GND**	A6	STORE_ALL	B6	A26	C6	LEVEL_1_BUSY*	D6	FAD2
Z7	**+5V**	A7	SYNCH_GAP	B7	A27	C7	LEVEL_2_BUSY*	D7	**GND**
Z8	**GND**	A8	DATA_READY*	B8	A28	C8	LEVEL_1_ERROR*	D8	FAD3
Z9	**+5V**	A9	**GND**	B9	A29	C9	**GND**	D9	**GND**
Z10	**GND**	A10	BC_Trig0	B10	A30	C0	BC_Trig1	D10	FAD4
Z11	**+5V**	A11	BC_Trig2	B11	A31	C1	BC_Trig3	D11	**GND**
Z12	**GND**	A12	BC_Trig4	B12	**GND**	C2	BC_Trig5	D12	FAD5
Z13	**+5V**	A13	BC_Trig6	B13	**+5V**	C3	BC_Trig7	D13	**GND**
Z14	**GND**	A14	**GND**	B14	D16	C4	**GND**	D14	FAD6
Z15	**+5V**	A15	**+5V**	B15	D17	C5	**+5V**	D15	**GND**
Z16	**GND**	A16	L1_ACCEPT	B16	D18	C16	TRST*	D16	FAD7
Z17	**+5V**	A17	L2_ACCEPT	B17	D19	C17	TDI	D17	**GND**
Z18	**GND**	A18	L2_REJECT	B18	D20	C18	TDO	D18	FAD8
Z19	**+5V**	A19	BC_CLOCK	B19	D21	C19	TMS	D19	**GND**
Z20	**GND**	A20	L3_HOLD	B20	D22	C20	TCLK	D20	FAD9
Z21	**+5V**	A21	TRGPROCENB	B21	D23	C21	EOD*	D21	**GND**
Z22	**GND**	A22	**GND**	B22	**GND**	C22	**GND**	D22	FAD10
Z23	**+5V**	A23	L2_MCEN_8	B23	D24	C23	L2_MCEN_0	D23	**GND**
Z24	**GND**	A24	L2_MCEN_9	B24	D25	C24	L2_MCEN_1	D24	FAD11
Z25	**+5V**	A25	L2_MCEN_10	B25	D26	C25	L2_MCEN_2	D25	**GND**
Z26	**GND**	A26	L2_MCEN_11	B26	D27	C26	L2_MCEN_3	D26	FAD12
Z27	**+5V**	A27	L2_MCEN_12	B27	D28	C27	L2_MCEN_4	D27	**GND**
Z28	**GND**	A28	L2_MCEN_13	B28	D29	C28	L2_MCEN_5	D28	FAD13
Z29	**+5V**	A29	L2_MCEN_14	B29	D30	C29	L2_MCEN_6	D29	**GND**
Z30	**GND**	A30	L2_MCEN_15	B30	D31	C30	L2_MCEN_7	D30	FAD14
Z31	**+5V**	A31	**GND**	B31	**GND**	C31	**GND**	D31	**GND**
Z32	**GND**	A32	**+5V**	B32	**+5V**	C32	**+5V**	D32	FAD15

Figure 2 — The J2 Connector

NC: Not connected

Signal Drivers and Receivers

Depending on the type and function of signals, we may need different families of drivers and receivers. The rules of thumb here are the following:

- Broadcasting signals need high current drivers / low current receivers
- Wire-Or signals are open collector or open drain.
- Daisy-Chain signals can be ordinary totem-pole.
- Point-to-point shared signals need to be tri-state.
- Special high-frequency (e.g. RF) clocks are in PECL.

PECL Signals

Four copies of the same signal, to distribute by different modules.

M_CLOCK+[3:0]
M_CLOCK-[3:0]

Standard Tri-State:

Must source 3mA, and sink 48 mA.

Typical Drivers: [LS] 645-1, 645A-1
Typical receivers: [LS, ALS, F] 240, 241, 244, EPLD
Transceivers: 645-1, 245a-1, 646-1, 648-1

AM[5:0]
D[31:00]
A[31:01]
IACK* (or Open-Collector)
WRITE*
LWORD*
RETRY*

High-Current Tri-State

Signals of High Edge Speeds
Must source 3mA, and sink 64 mA.
Typical drivers: [S,F] 241, 244
Typical receivers: [LS] 241, 244, EPLD

AS*
DS0*
DS1*

Standard Totem-Pole

Typical driver: Most LS, S, F, AS, ALS, PLDs
Typical receiver: Most LS, F, AS, ALS, PLDs

BG0IN*
BG1IN*
BG2IN*
BG3IN*
BG0OUT*
BG1OUT*
BG2OUT*
BG3OUT*
IACKIN*
IACKOUT*

High-Current Totem-Pole

Can be replaced by high-current tri-state if permanently enabled.

Typical driver: [S,F] 241, 244
Typical receiver: [LS] 240, 241, 244, EPLD

BCLR*
SYSCLK
SERCLK (SERA)

MASTER_RESET
STORE_ALL
SYNC_GAP
BC_TRIG[7:0]
RESET_COUNTERS
L1_ACCEPT
L2_ACCEPT
L2_REJECT
BC_CLOCK
L3_HOLD

TRST* (unbuffered)
TD I(unbuffered)
TMS (unbuffered)
TCK (unbuffered)

Open Collector

Typical driver: [LS, F] [38, 641-1, 642-1, 642-1]
Typical receiver: [LS], 14, 240, 241, 244, EPLD

ACFAIL*

BBSY*
BERR*
BR0*
BR1*
BR2*
BR3*
DTACK*
IACK*
IRQ1*
IRQ2*
IRQ3*
IRQ4*
IRQ5*
IRQ6*
IRQ7*
SERDAT (SERB)
SYSFAIL*
SYSRESET*

DATA_READY*
L1_BUSY*
L2_BUSY*
L1_ERROR*
EOD*

TDO (unbuffered)