<table>
<thead>
<tr>
<th>Year</th>
<th>Stage</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>Demonstrator</td>
<td>- Limited scope&lt;br&gt;- 1&lt;sup&gt;st&lt;/sup&gt; priority: functional test of requirements&lt;br&gt;- 2&lt;sup&gt;nd&lt;/sup&gt; priority: hardware implementation&lt;br&gt;- Integration: Fall 2000</td>
</tr>
<tr>
<td>2001</td>
<td>Prototype</td>
<td>- Hardware implementation is a priority&lt;br&gt;- Full channel count&lt;br&gt;- Integration: Fall 2001</td>
</tr>
<tr>
<td></td>
<td>Pre-production Prototype</td>
<td>- Production cloned from these&lt;br&gt;- Integration effort not necessary&lt;br&gt;- Completed: Summer 2002</td>
</tr>
<tr>
<td></td>
<td>Final Cards</td>
<td>- Begins: Fall 2002&lt;br&gt;- Duration 4-6 months&lt;br&gt;- Completed: Spr 2003</td>
</tr>
<tr>
<td></td>
<td>Installation</td>
<td>- Begins: Fall 2004&lt;br&gt;- Alcove Tests</td>
</tr>
</tbody>
</table>

Contingency
USCMS HCALTriDAS
Current Project Timeline

2001
- Demonstrator
  - Limited scope
  - 1\textsuperscript{st} priority: functional test of requirements
  - 2\textsuperscript{nd} priority: hardware implementation
  - Integration: Fall 2000

- Prototype
  - Hardware implementation is a priority
  - Full channel count
  - Integration: Fall 2001

2002
- Pre-production
  - Production cloned from these
  - Integration effort not necessary
  - Completed: Summer 2002

2003
- Final Cards
  - Begins: Fall 2002
  - Duration 4-6 months
  - Completed: Spr 2003

2004
- Installation
  - Begins: Fall 2004

Contingency
- Alcove Tests

Boston University. 11-Apr-01
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Schedule Slippage

• We are about 6 months behind relative to Lehman00

• Deadline of production cards coming in by late 2002 is still feasible
  – We will make pre-production cards sufficient for Alcove tests
  – Will allow us to find any bugs and maybe service any design change requests 😞

• What will have to be reduced?
  – Prototype stage
    • Change from 1 year to 6 months
  – Pre-production stage
    • Change from 1 year to 3 months
  – Ongoing software/firmware development for integration/commissioning
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Prototype/Production Phase

• Depends a lot on what link we use
  – If GLINK: “already” debugged and understood (at 40MHz)
    • Maybe also at 80MHz
    • Need to do studies (digital, analog, BER, etc)
  – If NOT GLINK:
    • Need to start another board ASAP to understand new technology
    • Schedule and cost implications
      – Tullio is already busy!
      – Not in the budget

• Depends on 40MHz vs. 80MHz
  – (or in other words, 2 chan/fiber vs. 3 chan/fiber)

• Any other increase in tasks?
  – FNAL source tests were not considered in Lehman00
Data transmission into HTR
  - Glinks 40 vs. 80 MHz
    • 80MHz ok, but only if it works SOON
  - Other technology?
    • Vitesse, Cypress, TI all make 8B/10B transceivers….
      - TI’s TLK1501, does 8B/10B presenting 16 bits data @ .6 to 1.5 Gbps
      - Requires another I/O board to be built and debugged.
      - We would need to figure out how to do this.
      - Can be done, but we would probably need more engineering.
      - We would do this at UMD, NOT FNAL!

Production assembly line
  - I did not fully appreciate the difficulty of checking out ~500 cards!
  - We need to plan how this is going to happen…
    • Pay some company? Probably too expensive, we don’t think this would work
    • Do it at UMD? Need to get going.
    • Do it at FNAL? Might make more sense….
  - We do not yet have a plan for this but will work on it with help….
Lehman estimate:
- $2.5k/card
- BUT I left out the following:
  - Optical connectors and detectors for feeding deserializer chips
- What do they cost?
  - Demonstrator boards use Stratus (Methode), cost $100/pair in quantity
  - For 16 channels, this is an additional $800
- What are the alternatives?
  - *e.g.* Infinion (or Infinio-like) Parallel Optical Link (PAROLI)
    - 12-channel connectors/detectors
    - 1.6 Gb/sec
    - Cost for ~500 Rx $476 each, 40-52 week lead time
      - Today’s price, quote from AVNET
  - More and more companies are getting into this
- Long lead times, etc, means that we need to have this decided NOW
  - Certainly by this fall

<table>
<thead>
<tr>
<th>Item</th>
<th>Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA (4 per card)</td>
<td>$1,000</td>
</tr>
<tr>
<td>PC Board</td>
<td>$200</td>
</tr>
<tr>
<td>Fab/Assy</td>
<td>$200</td>
</tr>
<tr>
<td>Connectors</td>
<td>$200</td>
</tr>
<tr>
<td>Misc (FIFOs, MUX, VME, etc.)</td>
<td>$400</td>
</tr>
<tr>
<td>Rx (16 @ $30 + Vitesse + LVDS...)</td>
<td>$500</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>$2,500</strong></td>
</tr>
</tbody>
</table>
USCMS HCAL TriDAS
HTR M&S Costs 40MHz v 80MHz

<table>
<thead>
<tr>
<th>Item</th>
<th>12fibers/2 chan</th>
<th>8fibers/3 chan</th>
<th>16 fibers/2 chan</th>
<th>16fibers/2 chan</th>
<th>12 fibers/3 chan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame clock (MHz)</td>
<td>40</td>
<td>80</td>
<td>40</td>
<td>40</td>
<td>80</td>
</tr>
<tr>
<td># Channels</td>
<td>24</td>
<td>24</td>
<td>32</td>
<td>32</td>
<td>36</td>
</tr>
<tr>
<td>Channels/FPGA (# FPGA)</td>
<td>8,8,8 (3)</td>
<td>9,9,6 (3)</td>
<td>8,8,8,8 (4)</td>
<td>N/A</td>
<td>9,9,9,9 (4)</td>
</tr>
<tr>
<td>FPGA 20k400 (large uncert’s)</td>
<td>$450</td>
<td>$450</td>
<td>$600</td>
<td>$1000</td>
<td>$600</td>
</tr>
<tr>
<td>PC Board</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
</tr>
<tr>
<td>Fab/Assy</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
</tr>
<tr>
<td>Connectors</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
<td>$200</td>
</tr>
<tr>
<td>Misc (FIFOs, MUX, VME, etc.)</td>
<td>$400</td>
<td>$400</td>
<td>$400</td>
<td>$400</td>
<td>$400</td>
</tr>
<tr>
<td>Rx @ $36</td>
<td>$432</td>
<td>$288</td>
<td>$576</td>
<td>$480</td>
<td>$432</td>
</tr>
<tr>
<td>Vitesse + LVDS…</td>
<td>$50</td>
<td>$50</td>
<td>$50</td>
<td>$20</td>
<td>$50</td>
</tr>
<tr>
<td>PAROLI ($40/fiber)</td>
<td>$480</td>
<td>$320</td>
<td>$640</td>
<td>0</td>
<td>$480</td>
</tr>
<tr>
<td>Total</td>
<td>$2,400</td>
<td>$2,100</td>
<td>$2,900</td>
<td>$2,500</td>
<td>$2,600</td>
</tr>
</tbody>
</table>

- Lehman 00 cost estimate increases by $400/HTR card
  - Still only an estimate – 25% contingency?
- 80MHz (3 channels/fiber)
  - Definitely cheaper
  - 12 fiber config – same cost as Lehman
  - 8 fiber config – much cheaper
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HTR Cost Comparison

- Baseline Lehman00:
  - 40MHz @ 32channel/HTR increase $200k
  - Costs estimates will change when we place orders!
    - FPGA, PAROLI, etc.
  - 32chan/card x 18 cards = 576 chan/crate – DCC can handle?
- Cost vs risk
  - 80MHz reduces cost, increases risk, and DCC cannot handle @ 36chan/HTR
  - 40MHz reduces risk
    - ~$100k increase in cost over baseline (16 fibers/HTR)
- This does NOT include FIBER CABLE PLANT COSTING!
- Note on PAROLI:
  - There may be serious implications as to how the fibers are bundled going into the HTR...

<table>
<thead>
<tr>
<th>Item</th>
<th>2/24 (40MHz)</th>
<th>3/24 (80MHz)</th>
<th>3/30 (80MHz)</th>
<th>2/32 (40 MHz)</th>
<th>3/36 (80 MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HTR Cards</td>
<td>$2.4k</td>
<td>$2.1k</td>
<td>$2.4k</td>
<td>$2.9k</td>
<td>$2.9k</td>
</tr>
<tr>
<td>Number of HTR</td>
<td>617 - $1.58M</td>
<td>617 - $1.30M</td>
<td>494 - $1.19M</td>
<td>463 - $1.33M</td>
<td>413 - $1.12M</td>
</tr>
<tr>
<td>VME Racks/Crates</td>
<td>12/34 - $220k</td>
<td>12/34 - $220k</td>
<td>11/30 - $200k</td>
<td>11/30 - $200k</td>
<td>9/22 - $150k</td>
</tr>
<tr>
<td>DCC/HRC</td>
<td>40 - $570k</td>
<td>40 - $570k</td>
<td>35 - $500k</td>
<td>35 - $500k</td>
<td>26 - $370k</td>
</tr>
<tr>
<td>Total</td>
<td>$2.39M</td>
<td>$2.09M</td>
<td>$1.94M</td>
<td>$2.03M</td>
<td>$1.74M</td>
</tr>
</tbody>
</table>
USCMS HCALTriDAS

“What is to be done?” – V. Lenin

• If 40MHz Glink…
  • Will work
  • We will make our source calib, test beam, and production milestones

• If 80MHz 8B/10B…
  • Might work but will definitely require more engineering/prototyping
  • With additional engineering we could definitely meet
    – Test beam, production milestones
  • Source calib milestone? No way. But we could consider:
    – Put CERN chip on HCAL front-end now.
    – Run as Glink for source calib using current demonstrator cards
      » Means we will have to make more of these
    – Switch front-end to 8B/10B for the rest of the project
  • Build HTRs with 12 fibers/3 channels per fiber
  • Might need to have more than 1 DCC per crate (additional $200k)
  • Be aware – still large contingencies for FPGA content of cost
  • We will be wasting money on HTR Glinks demonstrators

Remember…”it takes money to make money”
  – but keep in mind that 80MHz means we are still in R&D.
  – With 40MHz we are now heading out of R&D and into prototyping and integration