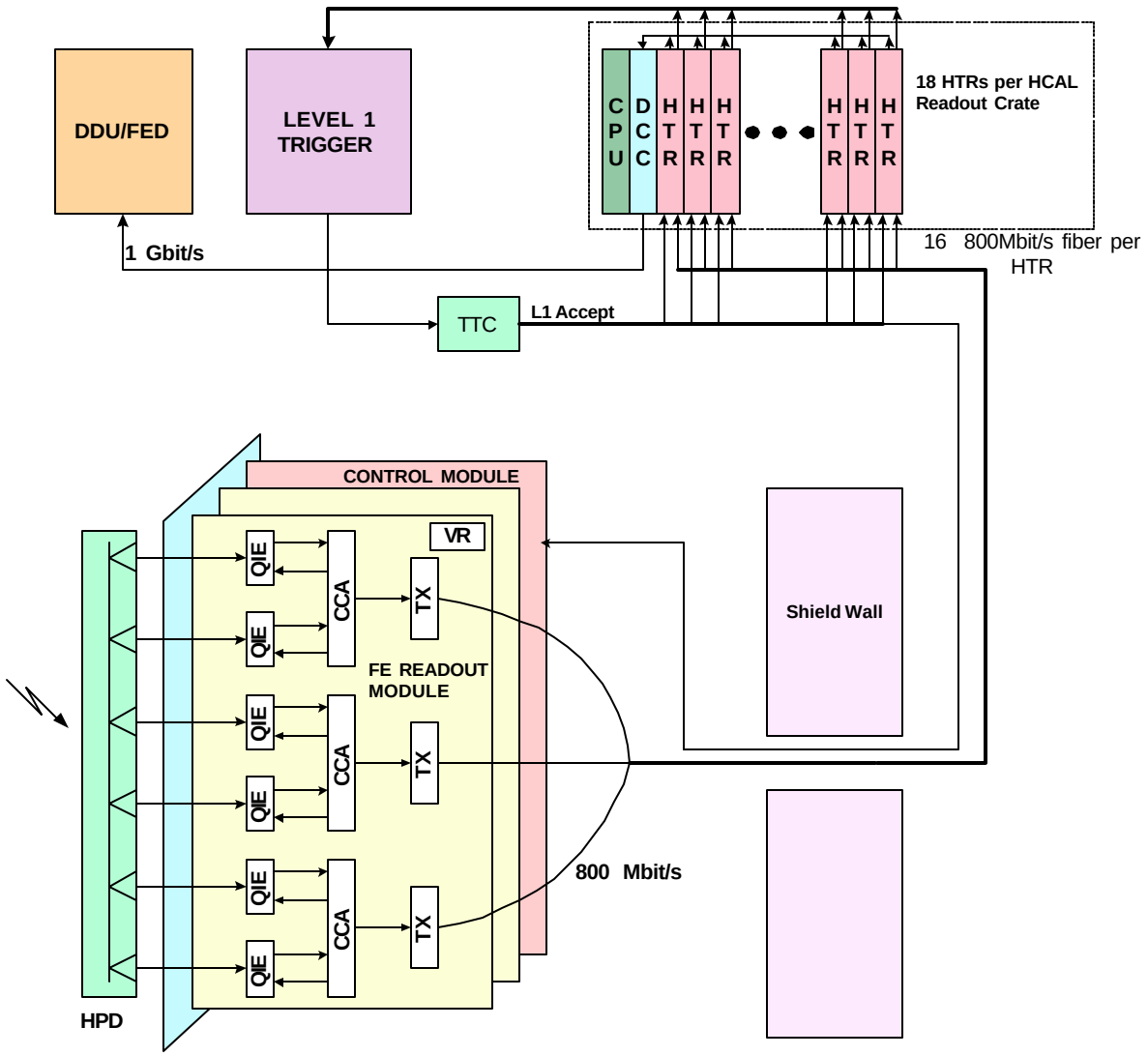
Electronics Overview

Electronics

- System Overview
- Power
- Backplane
- Readout Module (RM)
- Clock and Control Module (CCM)
- Calibration Module

Theresa Shaw
(FNAL)

FE/DAQ Readout



RBX Design Critical for Electonics

RBX

- Provides Power,
- Cooling,
- Clock distribution, and
- Slow Controls Communication

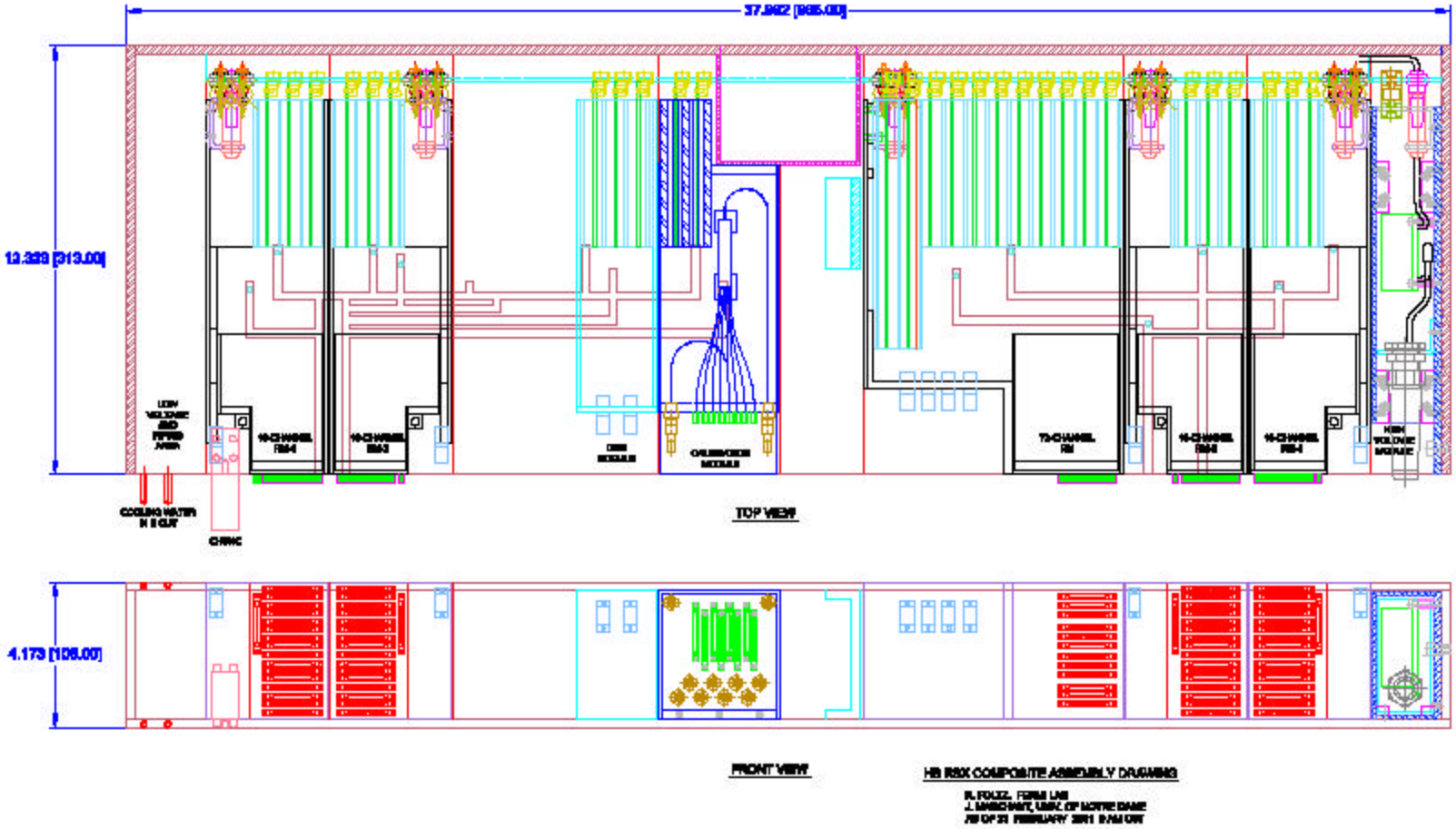
RBX Design critical for

- Connector Choice
- Backplane development
- Power/Grounding plans
- Prototype Work this Summer

HB RBX

36 HB RBXs

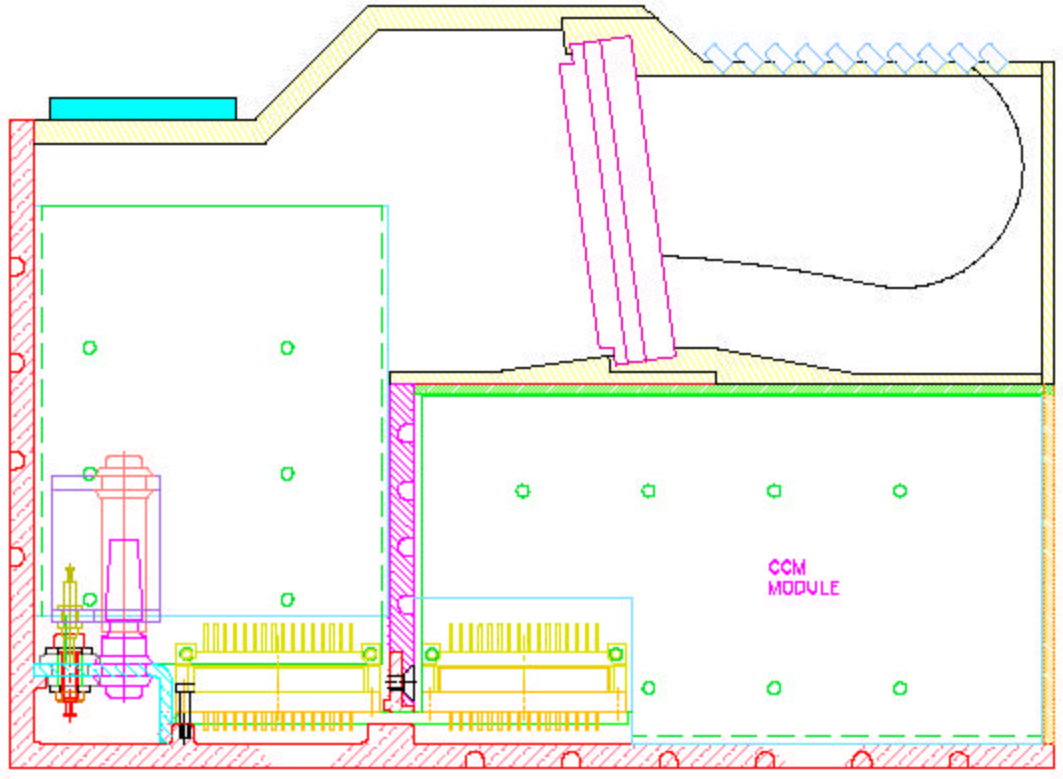
4968 Channels



HE Box

36 HE RBXs

3672 Channels



Power Consumption

Power Consumption

HB RBX – 298 W
23A@6.5V
33A@4.5V

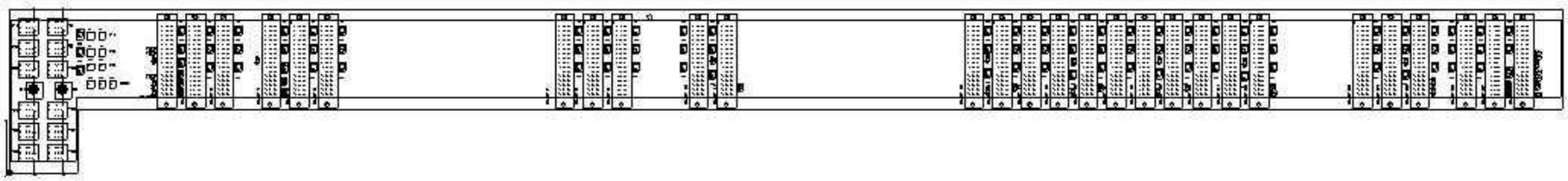
HE RBX – 205 W
17A@6.5V
21A@4.5V

			CURRENT and POWER at BOARD LEVEL										
FE Boards	QTY/BRD			POWER CONSUPTION					IDLING CURRENT				**TOTAL**
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	6		0.2	0.4									
CCA	3					0.3							
Serializer	3				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Board			0.265	0.505		0.897727							
Total Power / Board													**9.044773**
Calibration Module	(There are two boards per module)												
		VOLTAGE	5	5	2.5	3.3		5	5	2.5	3.3		
Chips													
QIE	3		0.2	0.4									
CCA	3					0.3							
Serializer	2				0.5								
LV regulat	3							0.025	0.025		0.025		
Current / Module			0.145	0.265		0.697727							
Total Power / Module													**5.804773**
CCM													
		VOLTAGE				3.3							
Chips						5							
LV regulators													
Current / Board						1.515152							
Total Power / Board													**6.818182**

HB Backplane Function

Backplane

- ~87 CM LONG
- Provides Power
- Distributes 40 MHz Clock (3 load max)
- Provides path for RBXbus (serial communication bus)
- Temperature feedback



Backplane Low Voltage Power Connector

Product Facts

"Inverse-sex" design meets IEC 950 safety requirements

Current rated at 7.8 amperes per contact, 23.5 amperes per module, fully energized

Sequenced right-angle headers available for "make-first/break-last" applications

ACTION PIN press-fit contacts on both headers and receptacle

Contacts designed for up to 250 mating cycles

Recognized to U.S. and Canadian requirements under the Component Recognition Program of Underwriters Laboratories Inc.

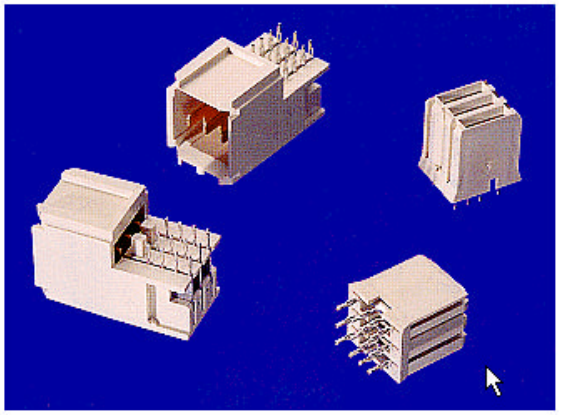
Low Voltage Distribution

3 Backplane Voltages

V1 (3 Universal Power Module Connectors for V1)
V2 (2 Universal Power Module Connectors for V2)
V3 (1 Universal Power Module Connectors for V3)
GND (6 Universal Power Module Connectors for GND)

Connectors allow for power sequencing

Universal Power Module



Backplane Connectors

Type C and Enhanced Type C Assemblies

Minimum adjacent mounting space required:

12.7 [.500]

Current Rating:

Per DIN 41612*

Voltage Rating:

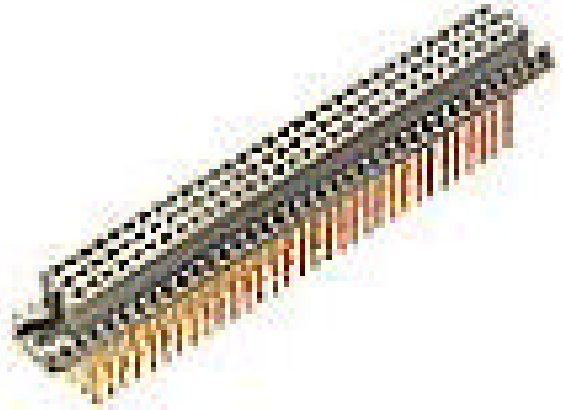
250 VAC

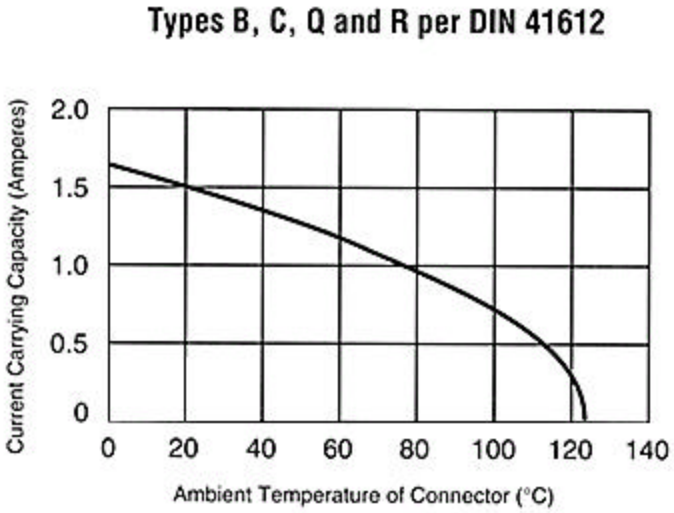
Dielectric Rating:

1000 VAC

Contact Resistance:

15 milliohms initial at 100 ma and 50 mv, open circuit



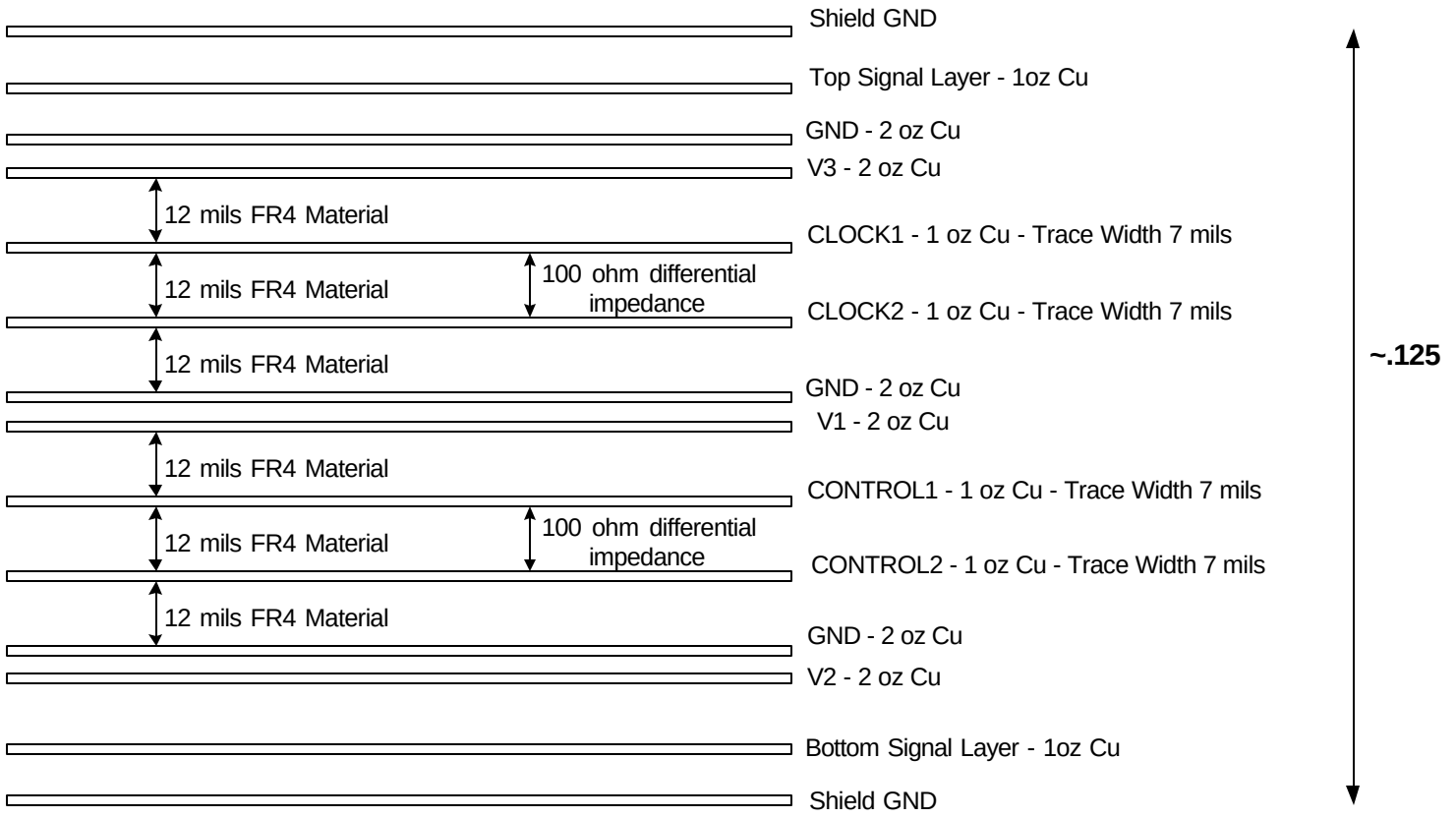


FE Card Pinout

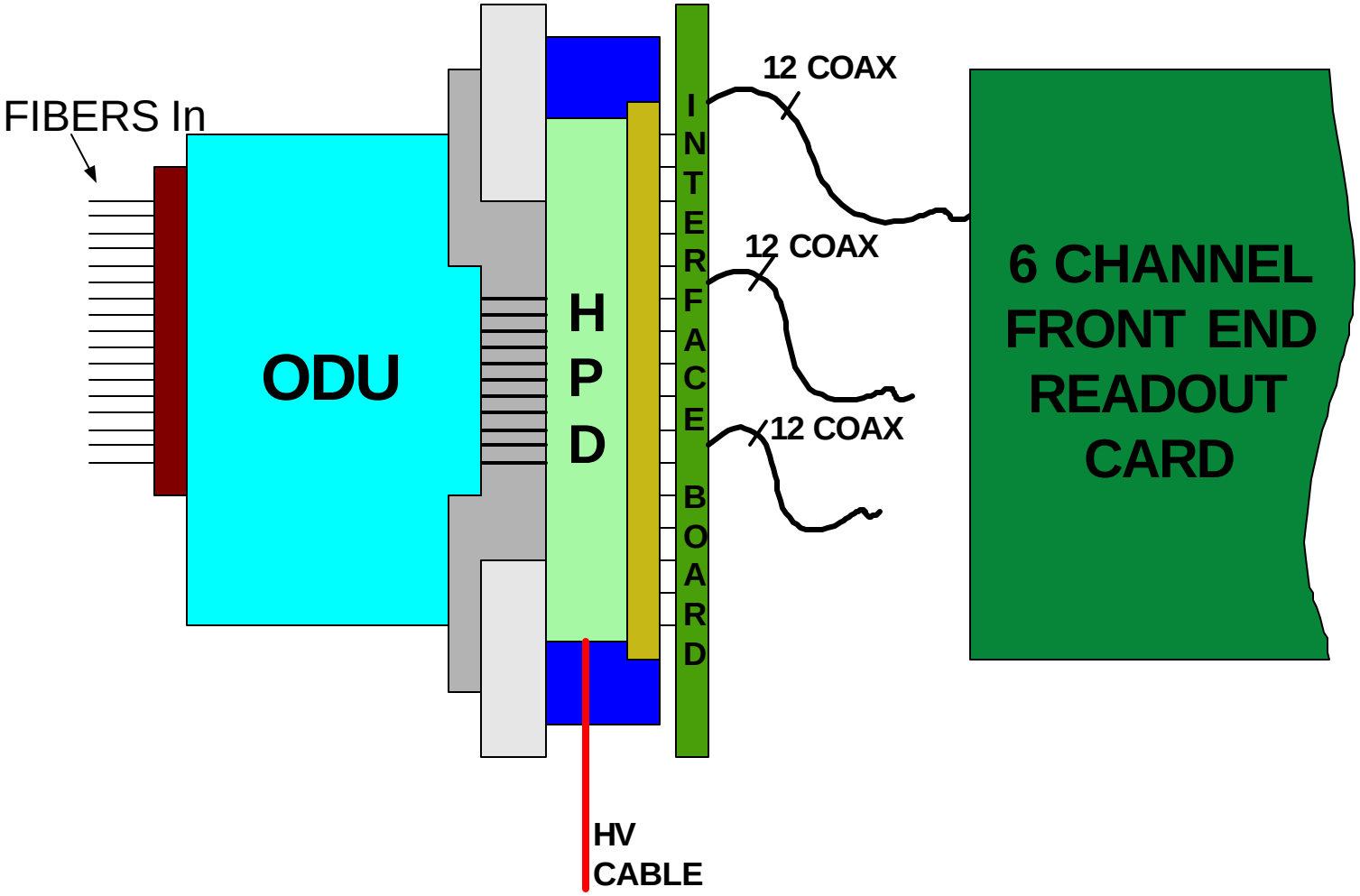
READOUT Card Slot

Pin Number	Row A	Row B	Row C
1	GND	GND	GND
2	V1	V1	V1
3	GND	GND	GND
4	V2	V2	V2
5	GND	GND	GND
6	V3	V3	V3
7	GND	GND	GND
8	MCLK+	D0_CALIB	RESERVED
9	MCLK-	GND	GND
10	GND	GND	TEMP
11	GEO_ADDR(0)	GND	GND
12	GEO_ADDR(1)	GND	RSVD(1)
13	RESET+	GND	RSVD(2)
14	RESET-	GND	SERCLK+
15	BZERO+	GND	SERCLK-
16	BZERO-	GND	SER_DAT

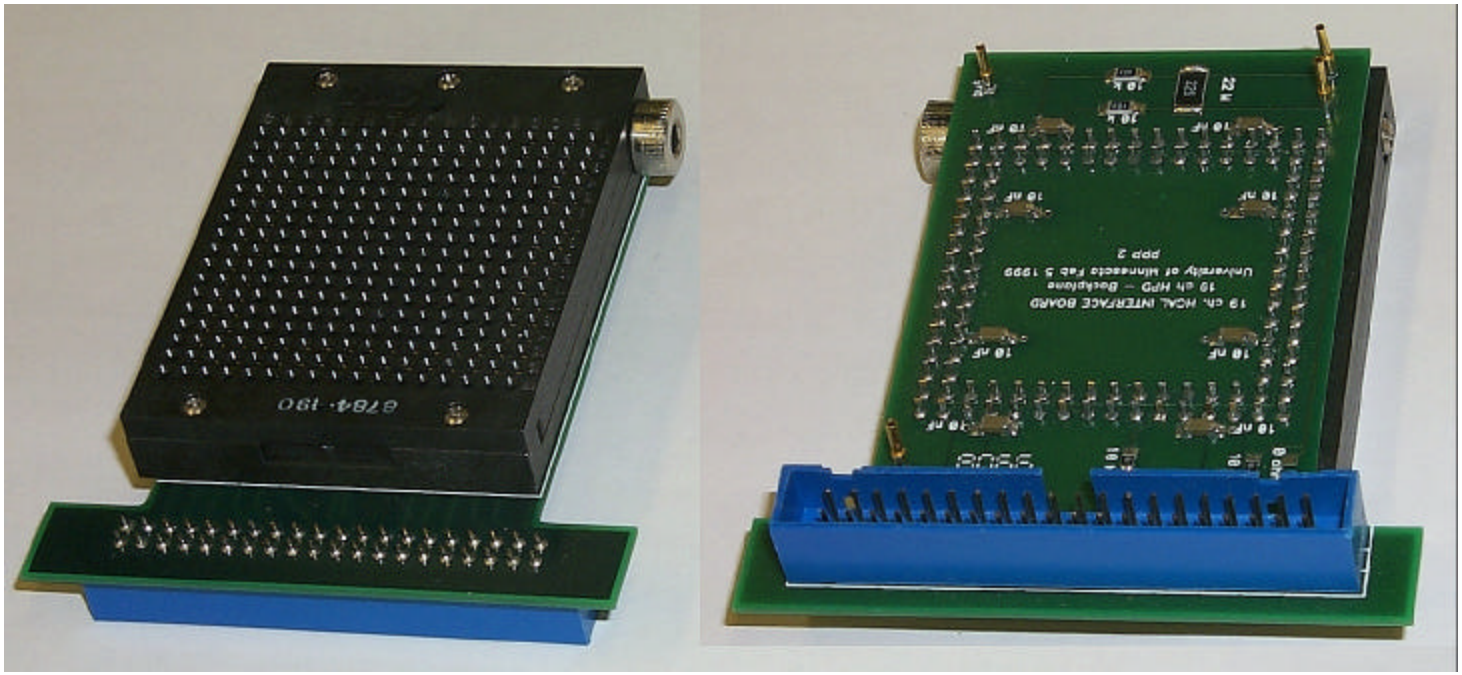
Backplane Stack-up



Readout Module Overview



HPD Interface Board

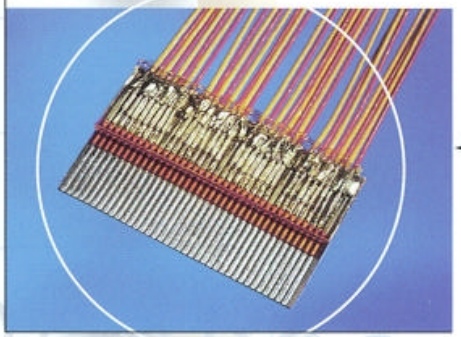


Signal Cable

PICO-FLEX®

OR USE PICO-FLEX :

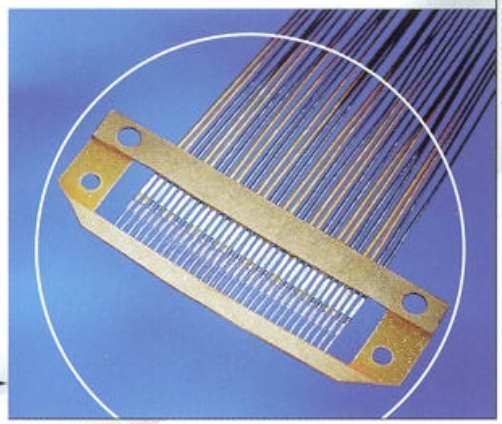
- Mounted in a ZIF connector surface mounted on a PCB.
- Available in 0,5 mm pitch (0,019").
- Compatible with PICO-COAX® AWG 40 to 46 (50 and 100 pF/m, 15 and 30 pF/ft).
- Custom designed versions available on request.



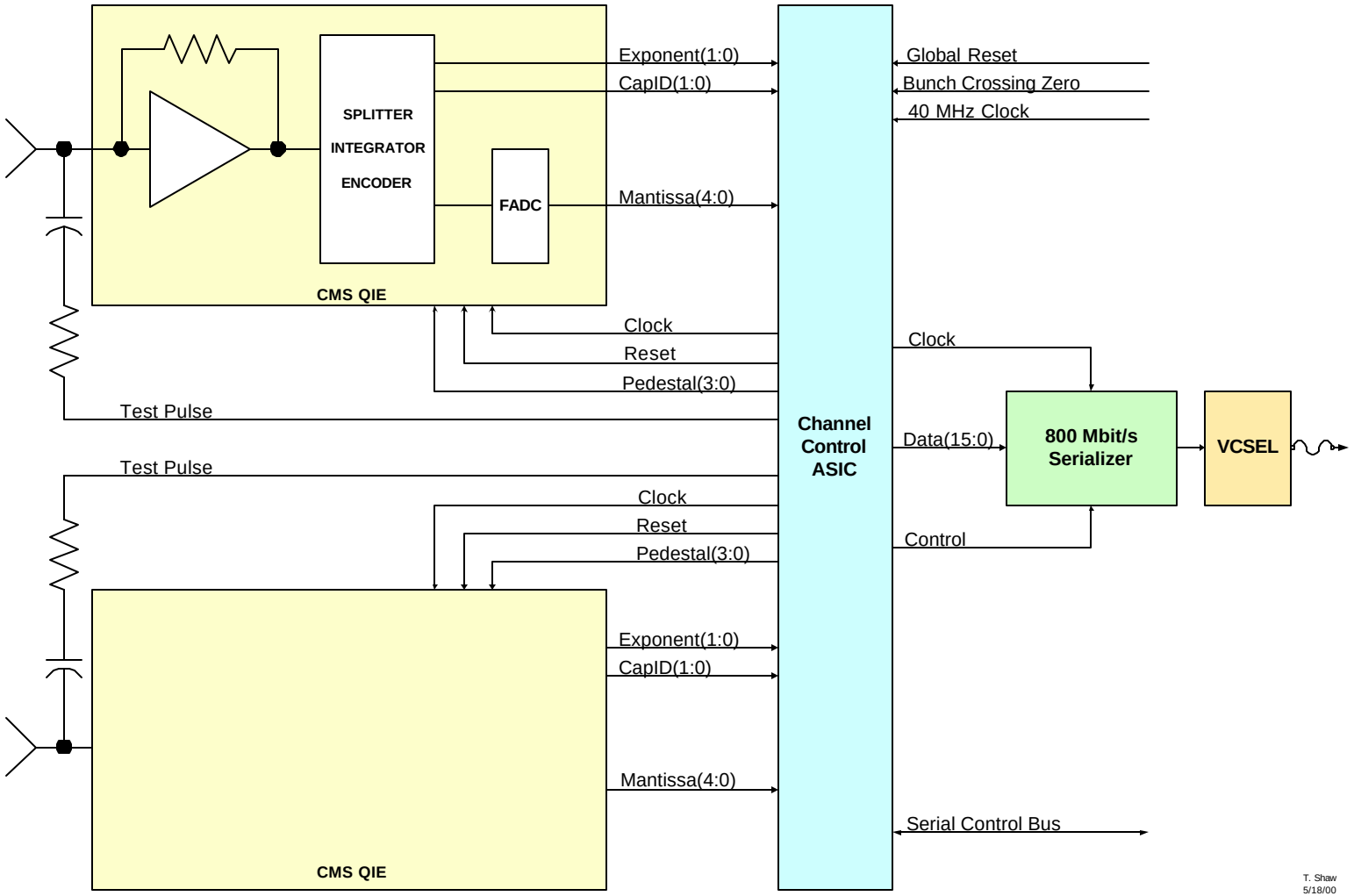
PICO-WELD®

USE PICO-WELD® :

- Solders directly to PC board.
- Maintains alignment of the PICO-COAX® at a constant pitch.
- Hot bar system soldering.
- Available in 32 positions pitch 0,635 mm (0,025").
- Compatible with AWG 40 and 42 (50 and 100 pF/m, 15 and 30 pF/ft).
- Other constructions available on request



FE Channels



CMS QIE Solution

QIE Description

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting and Non-inverting Inputs

Internal non-linear Flash ADC

Outputs

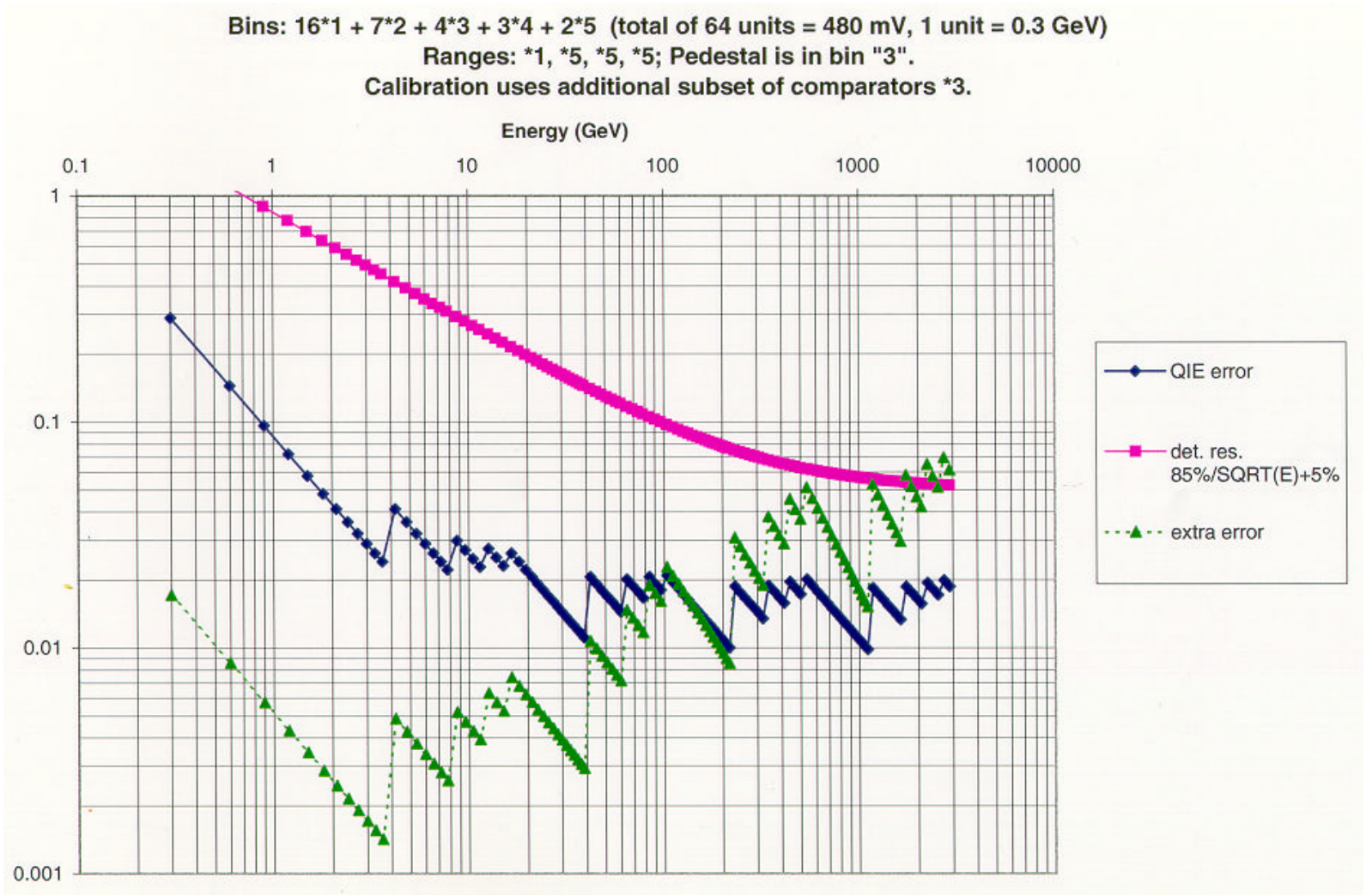
- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

QIE Specification

QIE Design Specifications

- Clock Speed >40MHz
- Must accept both polarity of charge input
  - Positive Input gain relative to Negative Input = 2.67
- Charge sensitivity Lowest Range = 1fC/LSB
  - In Calibration Mode 1/3 fC/LSB Range 0 only Linear FADC
- Maximum Charge = 9670 fC/25ns
- Noise 1.5 LSBs in calibration mode, gaussian
- Nominal Pedestal
  - Calibration Mode nominal Ped = 6.5
  - Normal Data Mode Ped = .5
- FADC Differential Non-Linearity < .05 LSBs

FLASH ADC Quantization



Channel Control ASIC

The CCA provides the following functions:

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

QIE/CCA Process Reliability

AMS 0.8u BiCMOS Process (QIE)

Early Failure rate 0.05 - 0.2%; can be reduced to a few ppm by burn-in

Predicted MTTF (25 sqmm, 55 C) is 1.67E8 hours

Expect less than 1 QIE failure per year

HP/Agilent 0.5u CMOS

Well established Commercial Process

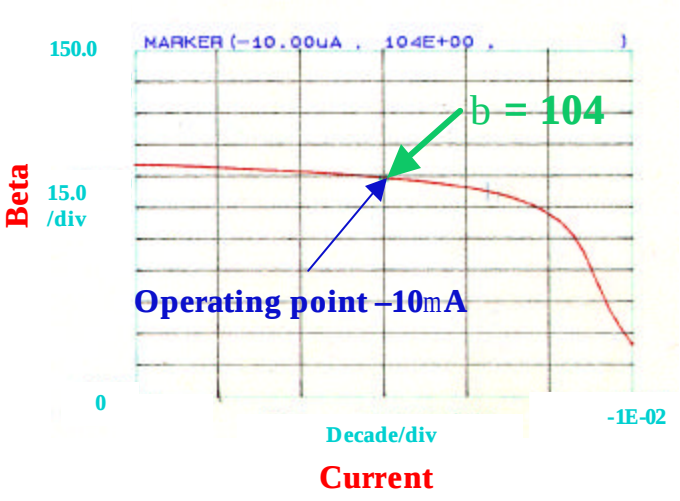
Radiation Tolerance

- **HCAL Radiation Environment**
  - **Radiation dose over 10yrs – 1kRad TID and 4E11 n/cm^2**
- **Electronics**
  - **QIE and CCA**
    - QIE – AMS 0.8 μm bi-CMOS process
      - **Test bi-polars (TID+bulk damage) and MOS circuits (SEU)**
    - CCA – HP 0.5 μm bulk-CMOS process
      - **Test MOS circuits (SEU)**
  - **Serializer – developed in rad hard process**
  - **LV regulators – developed in rad hard process**
  - **LEDs, other support components – need to test**
- **Studies performed at Indiana U. Cyclotron (200 MeV protons)**
  - **Bulk Damage studies**
    - Bi-polars dosed to fluence equivalent of 5E11 n/cm^2
  - **SEU studies**
    - AMS and HP test registers

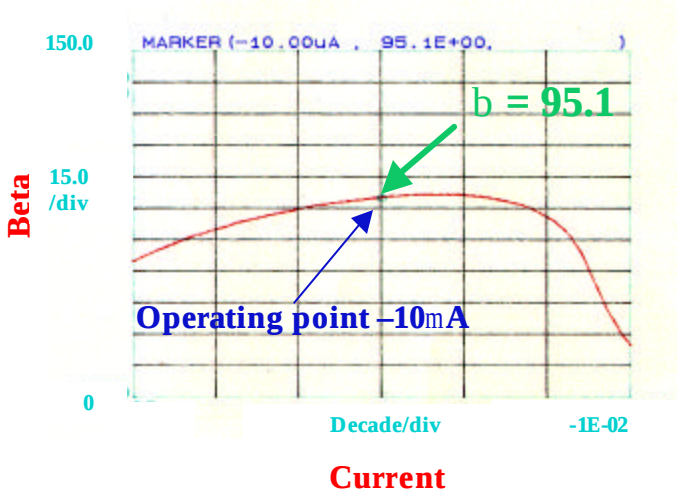
Bi-polar Radiation Studies for QIE

- **Bi-polars from AMS 0.8 μm bi-CMOS process**
  - **Beta for npn-transistors dropped by 5-10% after equivalent of 5E11 n/cm²**

Pre-irradiation



Post-irradiation (6 weeks)



SEU Studies for QIE and CCA

- **Test registers (min. feature size, min+guard ring, 2Xmin+guard ring, SEU tolerant)**
- **Xsec results for AMS and HP processes**
  - **(1-10)E-15 SEU per n/cm^2 per cell (depending on angle) for conservative design using 2Xmin feature size + guard ring**
- **For a complex ASIC with 1000 cells and a fluence of 4E11n/cm^2 over a 10 yr operating period**
  - **Expect .04-.4 of an upset per ASIC per year**

GOL Design Specifications

Synchronous (constant latency)

Transmission speed

- **fast: 1.6 Gbps , 32 bit data input @ 40 MHz**
- **slow: 0.8 Gbps , 16 bit data input @ 40 MHz**

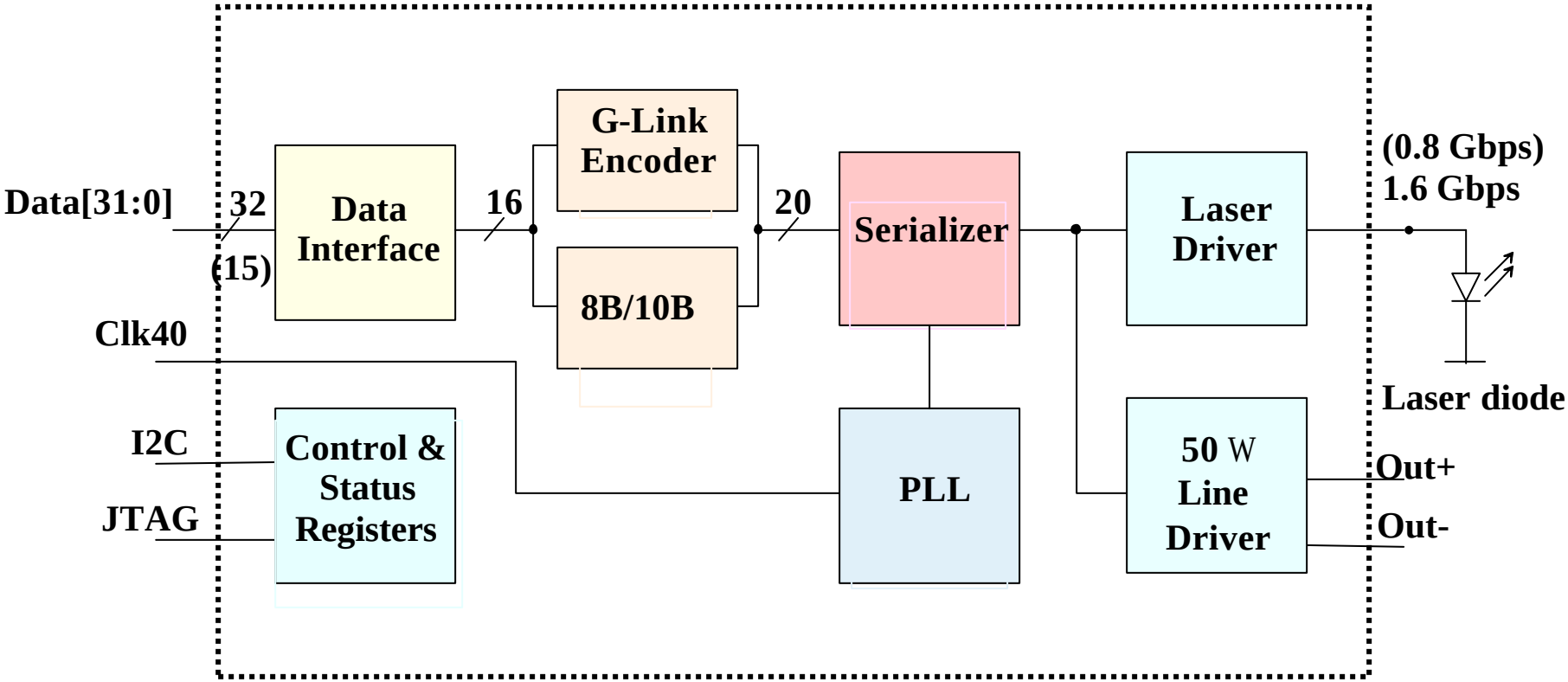
Two encoding schemes

- **G-Link**
- **Fiber channel (8B/10B)**

Interfaces for control and status registers

- **I2C**
- **JTAG**

Gigabit link (G-Link, 8B/10B optional)



GOL Radiation hardness

Deep submicron (0.25 um) CMOS

Enclosed CMOS transistors

Triple voting in state machines

Up-sizing of PLL components

Auto-error correction in Config. registers

Single Event Upsets

- Can we extrapolate for LHC?

CMS Environment	Pixel R = 4 – 20cm	Endcap ECAL R = 50 – 130cm	Tracker R = 65-120cm	Cavern R = 700 – 1200cm
Error/(chip hour)	$1.4\ 10^{-2}$	$1.9\ 10^{-4}$	$8.4\ 10^{-5}$	$3.1\ 10^{-8}$
#chips for one error each hour!	71	5.3K	12K	32M

VCSEL Selection

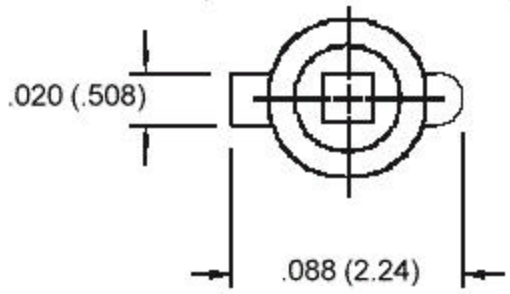
HFE4086-001

VCSEL Components, Data Communications, Flat Window Pillpack, Unattenuate optics, no back monitor photodiode

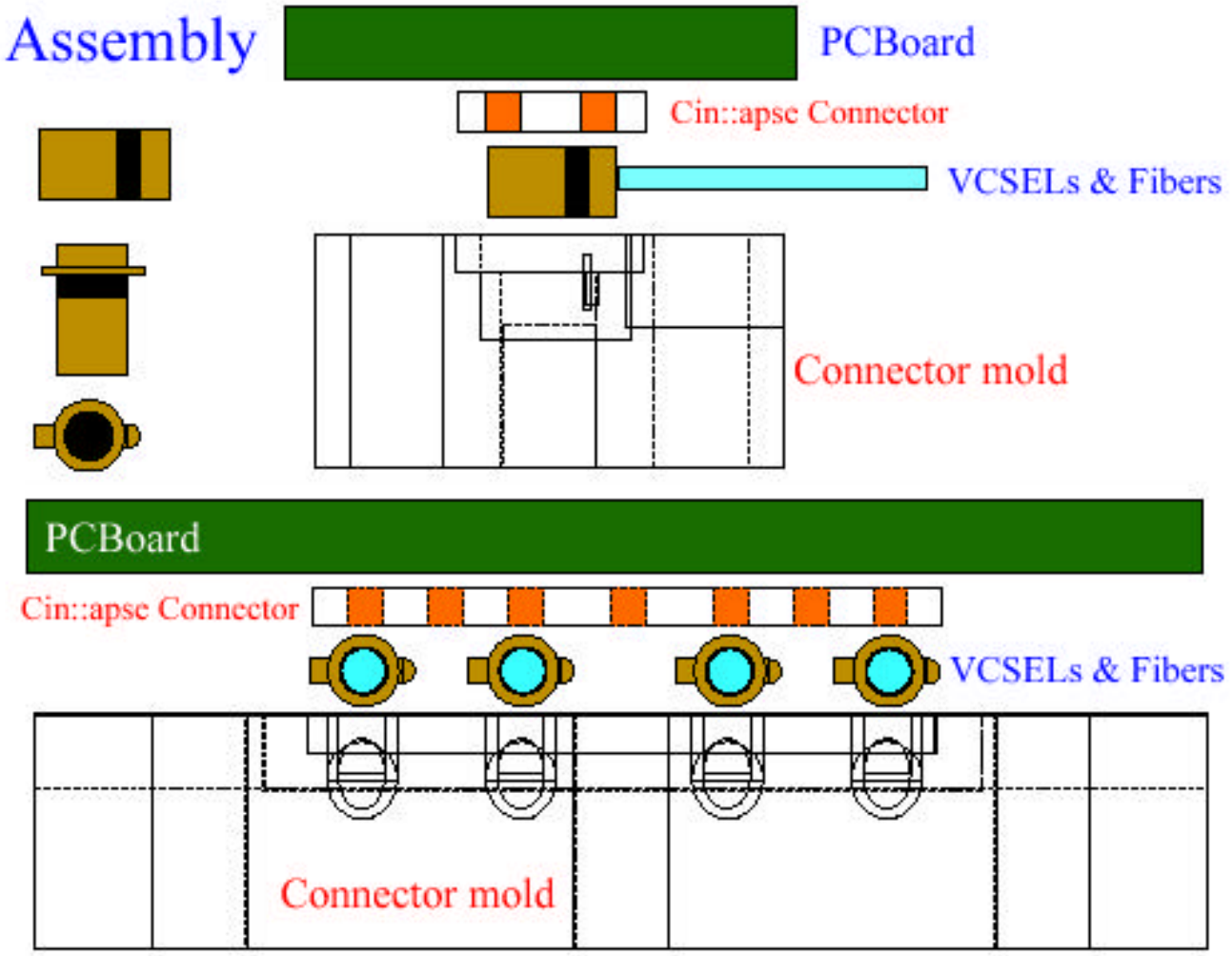
FEATURES

- Designed for drive currents between 5 mA and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz
- Miniature flat-window, pill-pack package

MOUNTING DIMENSIONS (for reference only): in./(mm)



VCSEL Mechanics



Rad Tolerant Voltage Regulator

Developed by ST Microelectronics

Specified by CERN RD49

Shown to be Rad Hard

Presently fixing overvoltage protection

Prepreduction parts due June 2001

Production parts late 2001

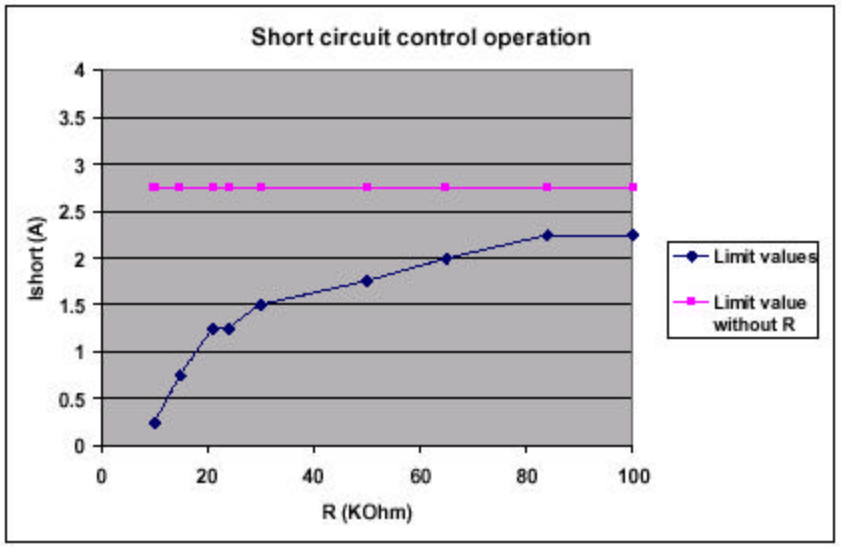
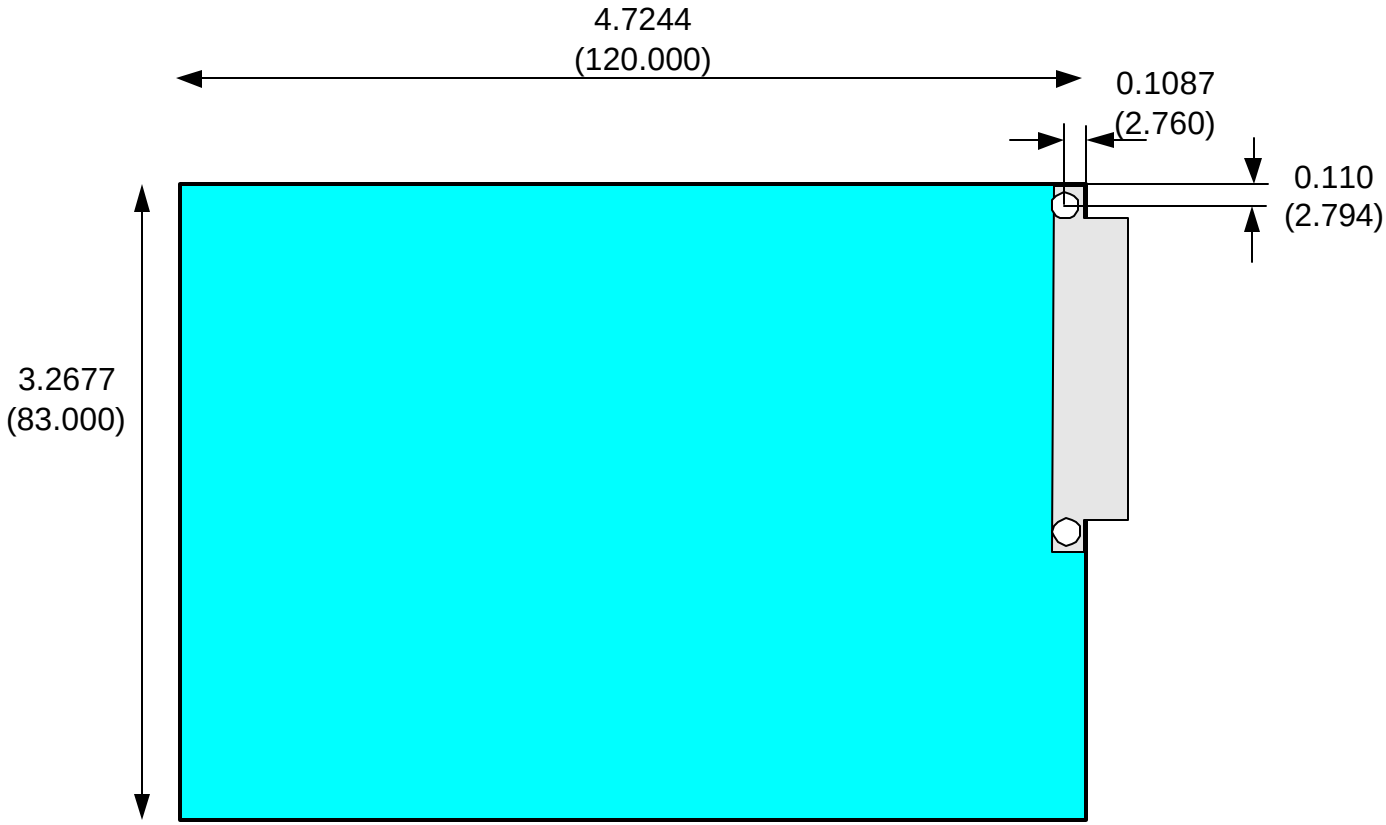
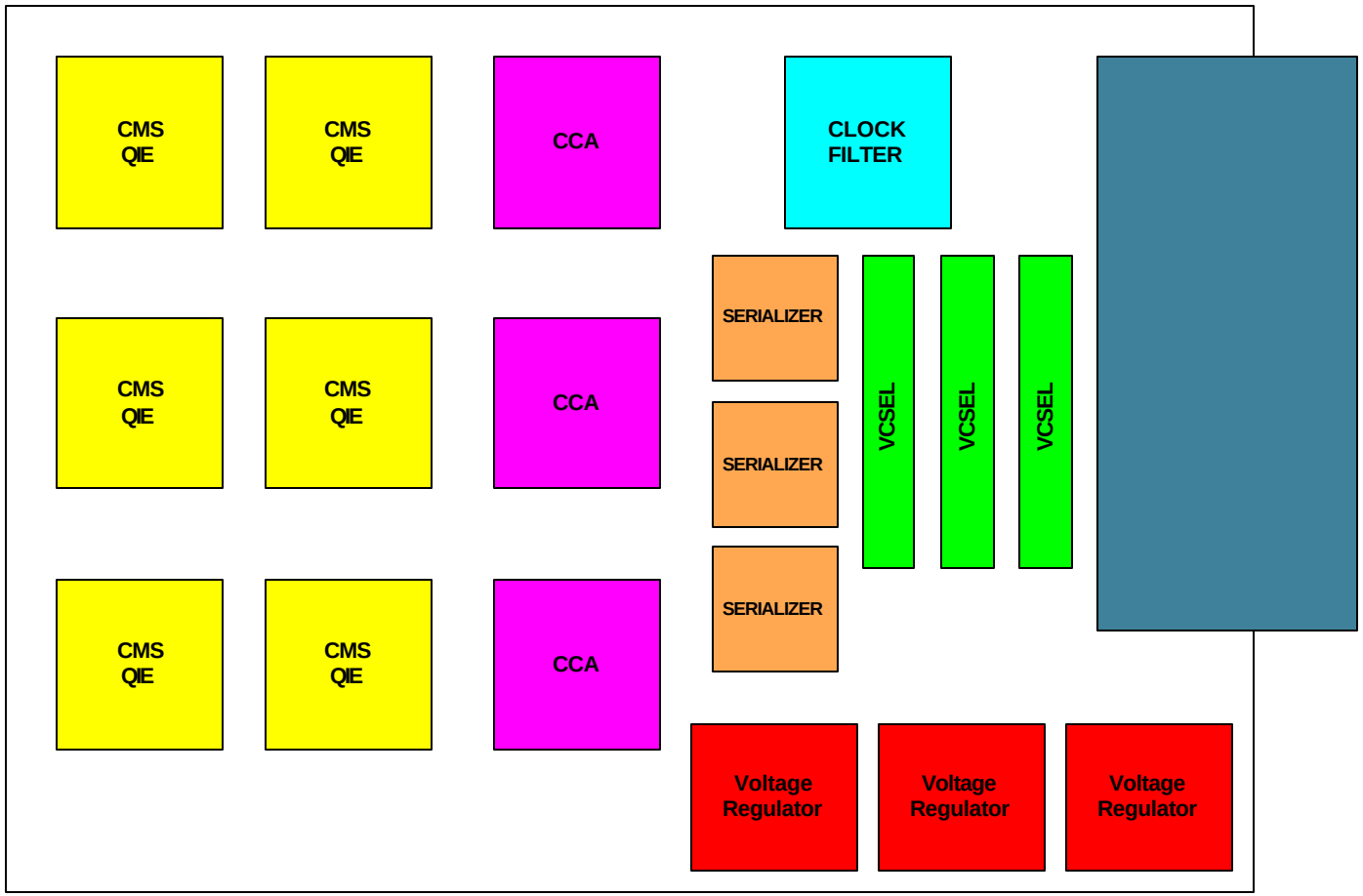


Fig. 7: Tuning of the maximum output current in a 2nd edition prototype regulator (version 2.5 V).

Readout Card Dimension

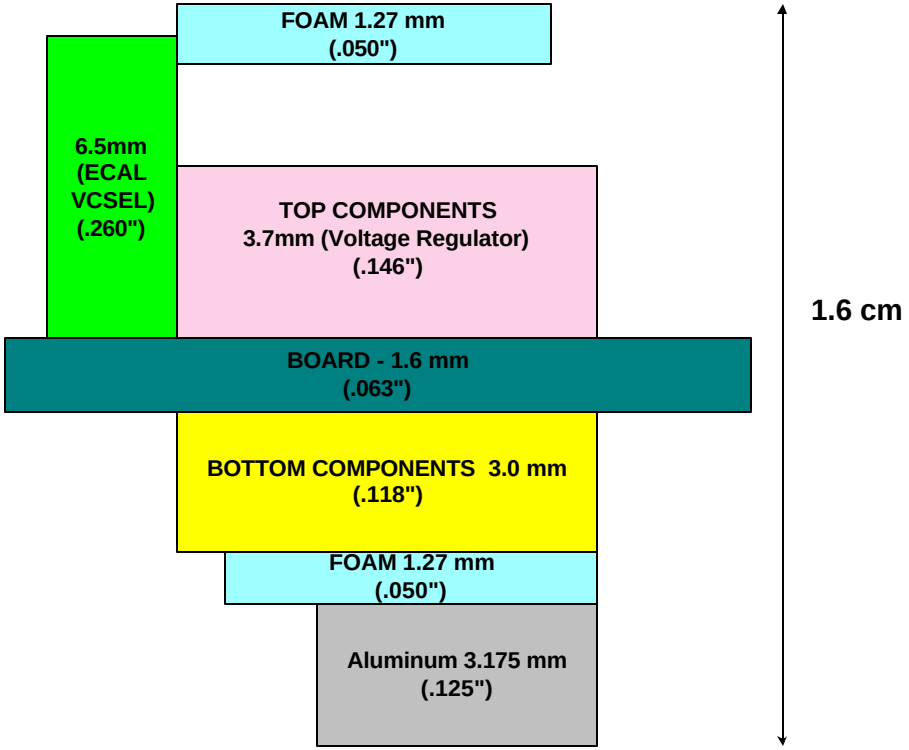


FE Card Component Area



Readout Card Component Height

Goal is 1.6 cm stack



Geometric Space For Components

Conclusions

Need to finalize RBX design

- Readout Card connector and mechanics cannot be finalized
- Backplane production on hold

Our Goal is to have a working FE/DAQ slice by Summer ’01

We would like to have a production RBX to test clock distribution, noise, …