NIM+ Development Project

Mohit Pandey[1] and Varun Ursekar[1]

[1]*Department of Physics, Boston University, Boston, Massachusetts 02215, USA*

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We test the latency time, decision time, minimum input pulse width, minimum input pulse height, and high-frequency performance of a programmable FPGA when used to detect two-channel signal coincidence. We test the FPGA using square-pulse generators and a pair of muon-detecting scintillators and compare the results with a standard LeCroy coincidence module.

INTRODUCTION

Nuclear Instrumentation Module (NIM) standard defines mechanical and electrical specifications for electronics modules, which is used in experimental particle and nuclear physics. The modular components designed to be inserted into common chassis ("NIM Crate") but it must be manually configured using knobs, cables and screwdrivers. This is a problem for modern experiments like the one at CERN which would benefit from flexibility and scalability beyond what NIM can provide. Also, it is hard to find spare parts or repair technicians for NIM. This is the motivation to upgrade NIM to NIM+.

Field Programmable Gate Arrays (FPGAs) are semiconductor devices that are based on configurable logic blocks, which are connected via programmable interconnects. Good thing about FPGAs is that they can be reprogrammed to desired application after it has been manufactured. The FPGA which we use for experiment is "ZedBoard"[2].

We test FPGA's capacity to perform a coincidence operation. We benchmarked it against a LeCroy coincidence module, which is a device commonly used in standard NIM crates. For this purpose, we implemented AND and OR operation in FPGA board. Given two input signals, an OR operation would give an output of 1 if either an input from signal A or signal B is measured by the device. An AND operation will would give an output of 1 if only if the device gets inputs from both signals A and B simultaneously.

EXPERIMENTAL SETUP AND PROCEDURE

The experimental setup in shown in Fig. 1. We first used Pulse Generator as our source of pulses. By passing one of the two signals through a Delay Generator, we get a signal delayed. We obtained two singlas of width 50 ns, which was delayed to about $5 - 30$ ns. After this, the signal was sent to a Level Adapter, which converts the signal to $+3V$ using a transistor-transistor logic (TTL). This is necessary because that's the operating voltage of ZedBoard. The pulse generators mimicked real sources, i.e. without noise, we used this to check for errors in our setup.

After we were sure, things were working well, we connected two parallel scintillator paddles to detect cosmic rays. It consisted of BisMSB blue scintillators, Lucite light waveguides and RCA 6342 fast PMTs, which was operated at 1000 Volts. Cosmic muons give pulses characterized by magnitude of $-100mV$.

We connect the PMT signal to a LeCroy Discriminator to get a square pulse of about $50ns$ and then we send it off to ZedBoard. We compared it to LeCroy coincidence module, which produces standard AND and OR pulses to compare with NIM+.

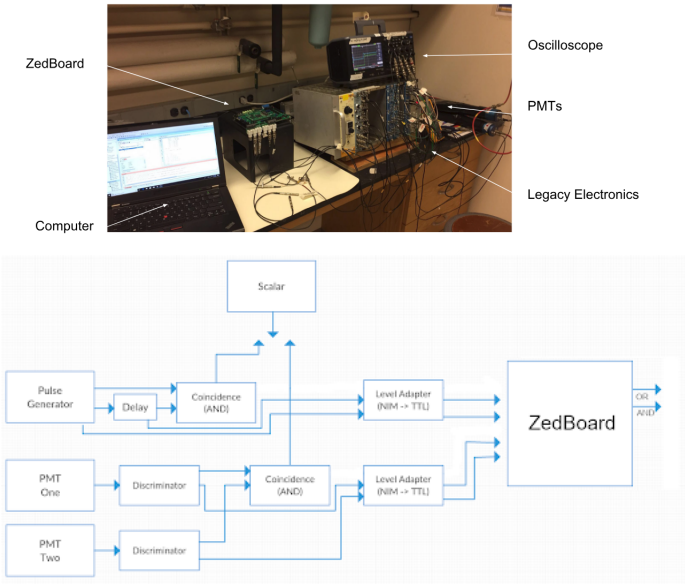

FIG. 1: Experimental Setup: Computer is connected to Zedboard that sends the code, Oscilloscope is used to look at signal , PMTs collects photons from scintillator, Legacy electronics contain Level Adapter etc. Image credit goes to Chris [1]

RESULTS

Our setup is able to correctly output AND or OR depending on signal A and B as shown in Fig. 2

We measure a few important statistics to evaluate the FPGA's performance

- Latency of Zedboard, which is defined as duration between leading edge of input and leading edge of output, with 50 ns pulse width for OR and AND was found:

$$L_t = 30 \pm 2\ ns \tag{1}$$

We find that the LeCroy coincidence module has a latency time of around

$$L_t = 15 \pm 2\ ns \tag{2}$$

This means that LeCroy processes signal faster than Zedboard.

- Decision time is defined as minimum overlap between 2 pulses to generate an output. For AND, we find decision time to be:

$$D_t = 5 \pm 1\ ns \tag{3}$$

- To test the minimum positive input pulse height that FPGA needs to process the signal, we inserted attenuators. An 80 % attenuation (2.4 V signal) still gives an output, while 50 % attenuation (1.5 V signal) does not. Hence, we expect that the actual cut-off must be within this range.

- We find that the smallest input width to be :

$$s_t \leq 5ns \tag{4}$$

- We find that the high rate performance is essentially optimal; we find that as long as frequency is not so high that signal starts overlapping for a given width, FPGA would output non-overlapping signal.

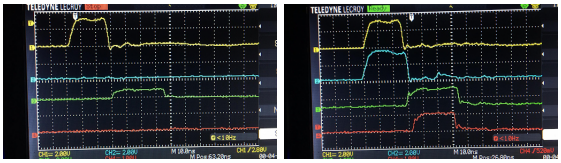

FIG. 2: From top to bottom: signal A, signal B, OR and AND. Left: Signal B is zero and that's why there is zero AND signal and non-zero OR signal. Right: AND signal corresponds to overlap between two signals. Image credit goes to Chris [1]

DISCUSSION AND CONCLUSION

There are two main fronts in which there is scope for improvement. First, the estimate for minimum input width should be improved by using a pulse generator with nanosecond precision. Second, it would be nice to implement a clocked version of the AND and OR operations. It would help in reducing the latency time of the FPGA.

ACKNOWLEDGEMENT

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[1] Chris Crosby. Review of nim+ project at bu cms testbench. 2018.
[2] Xilinx Website. http://zedboard.org.